Recent trends in the 200-Gb/s-class, 10-pJ/bit, compact, all-optical semiconductor gate devices research

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Abstract

After outlining our research backgrounds such as the recent growths in the numbers of optical-fiber-LAN subscribers in its leading countries Japan and Korea, we review recent results about the speed and energy consumption of ultrafast all-optical semiconductor devices (and about a few optical buffer memories from other institutes) under research, for use in ultrafast large-capacity optical network-node systems in the near future. One of the typical amount of dc-electric energy consumption has turned out to be about 5 pJ/bit in the 200-Gb/s all-optical gating operation, from our systematically characterized results with using existing III-V-semiconductor materials and devices from Japan, EU, and USA. Our standard experimental techniques for characterizing such semiconductor gates with precisely handling 200-Gb/s optical data signals are quickly introduced, too.

1. Introduction

It was December 1901 when Mr. Guglielmo Marconi and his colleagues succeeded in their transmit-and-receiving the mankind-first, wireless, binary-digital signals across the Atlantic Ocean.[1] In the last 107 years since that month, several big achievements from the electric-and-electronic *materials, devices, and systems* research have expanded our communication technology, and they are supporting the latest world-wide infra-structures of ours, 24 hours a day.

Recently, the demands in network systems' capacity and speeds are globally rising up. For instance, the number of optical-fiber-link subscribers in Japan has exceeded 10 millions in 2007 (Fig. 1).[2] In Korea and Japan, the numbers of optical-fiber-link subscribers per 100 inhabitants have reached nearly ten.[3] The optical-network capacities between wireless base stations have continuously been strengthened by our industry, too.
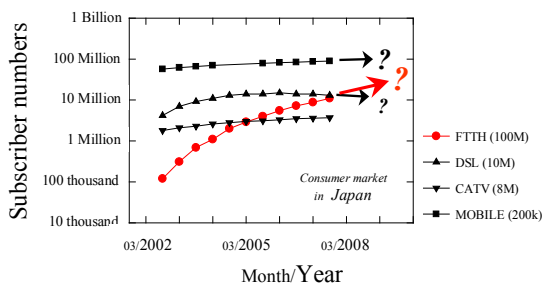
On the other hands in the world, the energy consumption of the numbers of large-scale ultrafast routers has started to appear as a bigger and bigger bottle-neck. One of the symbolic examples is the Cisco's new high-end router (Fig. 2) released in 2006-2007, which takes care of maximum 1,100 lines of optical 40-Gb/s signals (i.e., nominal through-put of 92-Tb/s). This system occupies about 70 of 2-meter-high heavy racks, and then consumes 1-MW electricity (and maybe even more electricity for air-conditioning its machine room).[4] The amount of electricity which Marconi was consuming for his transmitting his Morse-code signals across the Ocean in 1901 was, for comparison, supposed to be some tens of kW.

Fig. 2: A part of the Cisco's 92-Tb/s high-end router, CRS-1 (Ref. 4).

These two needs in front of us, that is, to enhance the capacity of network systems and to drop their energy consumptions will become stronger in the coming 10 years. With taking into account this on-going technological vision, several research institutes (most of which are located in Japan and Europe) have started intensively studying several groups of optical-signal-processing semiconductor devices (i.e., ultra-short clock-and-data generators, de-multiplexers, signal-wavelength converters, XOR gates, 3R regenerators, buffer memories, etc.) so that the extending research results will realize (a) faster, (b) lower-energy-consumption, and also (c) highly integrated network systems.

The transparent-transmission bandwidth of the recent standard silica-fiber cables ("wires") have already

Fig. 1: Numbers of broadband subscribers in Japan.[2]

reached a bandwidth wider than 100 THz as long as transmission distances of 10-20 km are concerned. These super-high-quality optical cables, working passively as ultrabroad-band communication waveguides, are already developed very well, very thin, and their operations need relatively little energy consumptions and fabrication costs, as has been known well. Even in the latest network systems, only 0.01-to-1 percentage (10-to-1,000 Gb/s) of the full 100-THz bandwidth per one connected-cable is efficiently utilized, being currently limited by the existing optical-and-electronic devices. What matters the most in the coming 10 years will be *what kind of signal processors* we will develop and start replacing the present network systems with that innovative technology.
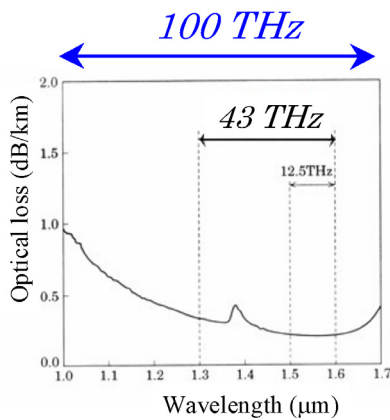

Fig. 3: Transparent transmission bandwidth (100 THz) of standard silica-fiber cables.

2. Speed and energy consumption of our fundamental optical signal-processors

In this talk, I will outline our recent studies on the speed and energy consumption of our all-optical semiconductor gates, for use as signal-processing units in future network-node systems.

In our research group in the Univ. of Electro-Communications, we are *not* crystal-growing nor fabricating semiconductor-crystal chip structures. Every year, instead, we (the grad- and undergrad-students) are building (a) proto-type all-optical semiconductor gates and some "circuits," (b) ultrahigh-frequency clock- and data-signal sources, (c) ultrahigh-resolution optical waveform- and spectrum-monitoring systems, (d) and other important experimental devices.

The semiconductor optical amplifier (SOA), in which the ultrafast and extremely efficient photon-electron interactions take place, is always the most important material in our building our all-optical gates.[5-8] In 2004-2006, for example, we discussed with and received several series of partially-customized research-level SOA chips from three leading institutes in Japan, EU, and USA, respectively, so that we can experimentally characterize them in addition to limited numbers of commercially-available butterfly-packaged SOA's.[9, 10]

Figure 5 shows a schematic view of the most fundamental all-optical-gate structure which we have currently been focusing on. Even though its number of all-optical functionalities in practical network-node systems has been supposed to be relatively limited (wavelength conversion,[5-8] optical 2R regeneration, etc.), this fundamental gate scheme has been playing the most powerful role in our design-and-characterization studies on these ultrafast semiconductor materials and devices. We believe that this will be one of the best gate schemes to further study fundamental principles of ultrafast optical materials and devices.
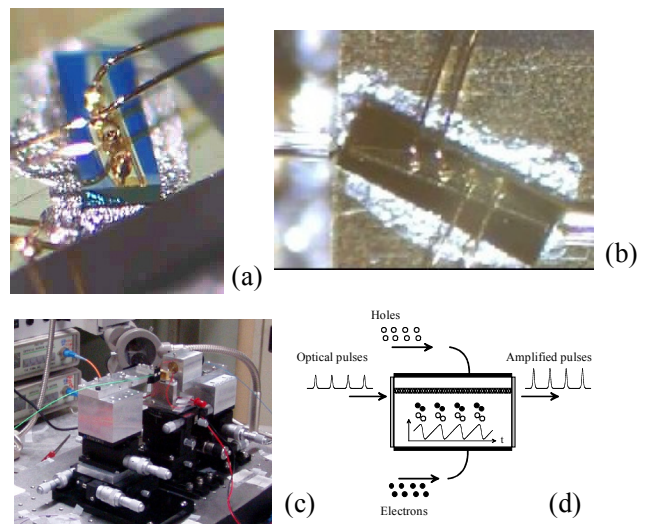

Fig. 4: Research-level SOA chips which are placed inside our all-optical gates and circuits. (a): microscope photo, (b) and (c): lensed-fiber-connections to the chip, (d) ultrafast photon-electron interactions inside the SOA's which drive our all-optical gates.
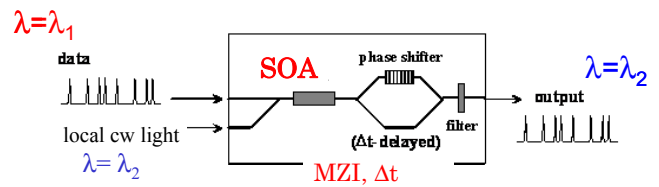

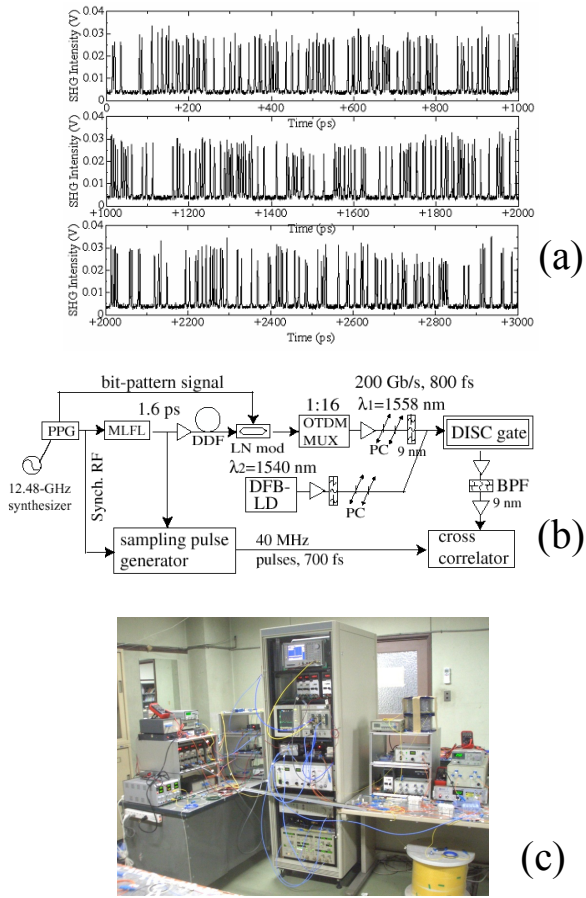Fig. 5: Schematic view of the most fundamental all-optical-gate structure.[5-8]

Fig. 6:   Ultrafast 200-Gb/s optical-data signal,
Experimentally generated in our lab.
(a)   Measured binary-encoded waveforms, (b) block
diagram of our home-made data-signal source and
all-optical waveform-monitoring system, (c) part of
our experimental setup.[10, 11]

Figure 6(a) shows one of the typical binary-encoded 1.55-μm-band, 200-Gb/s optical data signal's waveforms, experimentally generated in our laboratory.[10, 11] The distance between the adjacent two bits is adjusted to 5 ps, the width of each one-bit pulse is approximately 1 ps, and the length of encoded data pattern is 5,000 bits. The 1/16 seed pulses of this ultrahigh-frequency data signal is generated by a commercial, research-level mode-locked fiber laser and an adiabatic-soliton compressor, operating at the base frequency of 12.5 GHz in our laboratory. We are building and improving our ultrafast waveform-monitoring system. The high-precision, high-resolution all-optical waveform-monitoring system (Figs. 6(b) and 6(c)) was developed in our laboratory, too, and used in measuring the 200-Gb/s data signals such as those in Fig. 6(a).[10, 11] This monitoring system is sub-harmonically running at the 1:5,000 frequency (40 MHz) with respect to the data frequency (200 GHz). In the original scheme of ours in Fig. 6(c), the optical reference pulses required in the scheme are synchronously triggered by a train of short pulses from a commercial, research-level 40-MHz

mode-locked fiber laser.

Fig. 7 shows one of the experimental results that we achieved in May, 2008.[10, 11] Fig. 7(a) shows a part of the 200-Gb/s, 5,000-bit-long, binary-encoded data signal, generated in a manner similar to those in Fig. 6. We input this data signal to one of our home-made all-optical semiconductor gate which was schematically shown in Fig. 5. Figure 7(b) is the binary data signal measured at the output of the semiconductor gate. The measured waveform in Fig. 7(b) indicates that the speed of the semiconductor gate we used in this experiment is *as fast as* the speed of the data signal (200 Gb/s). From our experimental characterizations and analyses, we have recently understood that the speed of the semiconductor gate was strongly accelerated from 10-20 GHz up to 200 GHz up to now by three (i.e., one old and two new) significant physical factors.[7, 10, 11] Due to our understandings of these three physical factors, the quality of the gated 200-Gb/s data-signal waveform was dramatically improved from the previous poor one (which is not shown), to the significantly better one in Fig. 7(b).
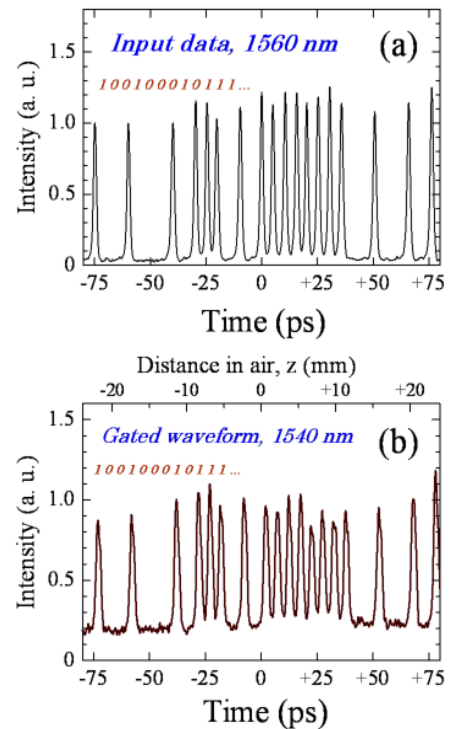

Fig. 7: 200-Gb/s optical-data signals.
(a)   Data signal (λ= 1560 nm), measured at the input of an all-optical gate, and, (b) wavelength-converted data signal (λ= 1540 nm), measured at the output of the all-optical gate.[10, 11]

The other important subject, the energy consumption of the all-optical semiconductor gate, has been studied as a function of the all-optical gating speed, along with our

above-mentioned 200-Gb/s gating experiments. The dc-electric energy consumption, which is originated from the dc-electric-bias-current injection into the SOA chip, has turned out to *increase linearly with* the optically accelerated gating speed (Fig. 8(a)).[9, 11] The typical numbers we obtained with the latest SOA-chip design were; 20-pJ/bit consumption in 200-Gb/s gating and 10-pJ/bit consumption in 100-Gb/s gating. When we adopted one of the two new acceleration factors to the all-optical gate, the energy consumption dropped from 20-pJ/bit to *below 5-pJ/bit* in the above-mentioned latest 200-Gb/s gating experiment in Fig. 7(b). This reduced level of dc-electric energy consumption approximately matches to that in the world-record-fast 320-Gb/s wavelength conversion experiment reported by Y. Liu, et al., from the Netherlands in Ref. 8. (Approximately 2×10^7 quantum electron-hole pairs are consumed per one bit.)

These levels of energy consumption that we have recently induced from our experimental research results with existing SOA chips seem to us to be not bad, as we had been expecting before them. First, the electric-energy-consumption levels of optical buffer memories, under separately on-going global research, are close to the above levels. The energy consumption level of a micro-ring memory reported by M.T. Hill, et al. in 2004, was 1 pJ/bit in its 25-Gb/s operation.[12] That of bistable VCSEL memory, reported by H. Kawaguchi, et al. in 2006, was 3 pJ/bit in its 10-Gb/s operation.[13] That of bistable PC/QD-SMZ-switch memory is expected to be less than 1 pJ/bit in its 10-to-40 Gb/s operation.[14] Second, the energy consumption of Cisco's CRS-1 router is 30 nJ per one-bit routing. That of the latest computer-CPU processors from Intel and AMD is 1 nJ per one instruction.[15] Beyond the existing practical applications in large-scale ultrafast network-node systems, depending upon the on-going research progresses in terms of the energy consumption of all-optical gates and buffer memories, researchers will finally be able in the near future to fabricate and demonstrate the mankind-first integrated optical-signal-processor chip in a manner similar to the historical Intel 4004 chip (Fig. 9) but, with performance 100 times faster than the latest Intel chip and without increasing its energy consumption.
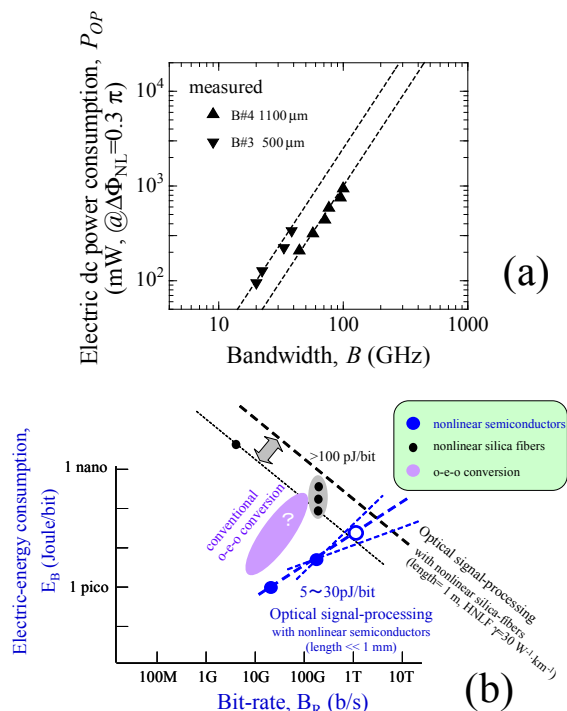

Fig. 8: Energy consumption of the all-optical semiconductor gate as a function of the optically-accelerated gating speed.
(a) Measured dc-electric power consumptions,
(b) comparisons with the alternative ultrafast devices, that is, the research-level ultrafast o-e-o devices and the research-level highly-nonlinear-fiber (HNLF) devices
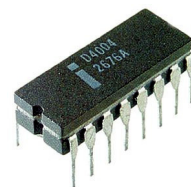

Fig. 9: Mankind-first integrated signal-processor chip, Intel 4004, released in 1971.
Clock frequency was 500 kHz. The energy consumption is unfortunately unclear. On the 3×4 mm^2 surface of a silicon chip, 2,300 transistor gates was integrated. 16 of 4-bit-long resister memories were included.

3. Other on-going topics

Within the range of our laboratory's on-going research activities, we have been exploring one of the potential applications of our all-optical gates, that is, experimental studies of ultrafast optical clock-pulse sources with using the all-optical gates.[16-18] Figure 10 shows one of the most recently achieved results.[18] In this series of experiments, a stable train of 10-GHz-repetition, 2-ps-long, single-longitudinal-mode, nearly-Fourier-transform-limited optical-clock-pulses was generated

from our original ring-laser-cavity scheme, which contains the all-optical semiconductor gate structure in a manner very similar to that in Fig. 5.

Separately from this talk, two other talks about closely related on-going research results will be given by their respective graduate students, in this year's symposium on Advanced Information and Communication Technology (AICT).[19, 20]
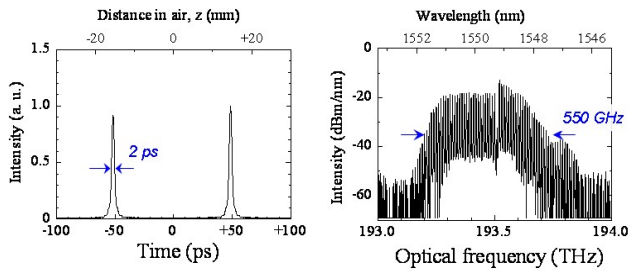

Fig. 10: 10-GHz, 2-ps, nearly-Fourier-transform-limited mode-locked pulses generated by our original ring-laser-cavity scheme that contains the all-optical semiconductor gate.[16-18]

References

1. Biography and Nobel lecture text of Guglielmo Marconi, Nobel Foundation , http://nobelprize.org/
2. Statistical data released by the Telecommunications Bureau (http://www.tele.soumu.go.jp/e/), the Ministry of Internal Affairs and Communications, Japan, on March 18, 2008.
3. Statistical data from the Organization for Economic Co-operation and Development (OECD), http://www.oecd.org/sti/ict/broadband/
4. Product brochure of the carrier routing system (CRS-1), October 2006, Cisco Systems, Inc., San Jose, CA, USA.
5. Yoshiyasu Ueno, Shigeru Nakamura, and Kazuhito Tajima, "Record low-power all-optical semiconductor switch operation at ultrafast repetition rates above the carrier cutoff frequency," Opt. Lett. vol. 23, no. 23, pp. 1846-1848, Dec. 1998.
6. Y. Ueno, S. Nakamura, and K. Tajima, 'Nonlinear phase shifts induced by semiconductor optical amplifiers with control pulses at repetition frequencies in the 40-160 GHz range for use in ultrahigh-speed all-optical signal processing,' J. Opt. Soc. Am. vol. B19, no. 11, pp. 2573-2589, Nov. 2002.
7. M.L. Nielsen, J. Mørk, R. Suzuki, J. Sakaguchi, and Y. Ueno, 'Experimental and theoretical investigation of the impact of ultra-fast carrier dynamics on high-speed SOA-based all-optical switches,' Optics Express, vol. 14, no. 1, pp. 331-347, Jan. 2006.
8. Y. Liu, E. Tangdiongga, Z. Li, Huug de Waardt, A. M. J. Koonen, G. D. Khoe, Xuewen Shu, Ian Bennion, and H. J. S. Dorren, "Error-free 320-Gb/s all-optical wavelength conversion using a single semiconductor optical amplifier," J. Lightwave Technol., vol. 25, no. 1, pp. 103-108, Jan. 2007.
9. Jun Sakaguchi, Ferran Salleras, Kohsuke Nishimura, and Yoshiyasu Ueno, "Frequency-dependent electric dc power consumption model including quantum-conversion efficiencies in ultrafast all-optical semiconductor gates," Optics Express vol. 15, no. 22, pp. 14887-14900, Oct. 2007.
10. Jun Sakaguchi, Takehiro Nishida, and Yoshiyasu Ueno, "200-Gb/s wavelength conversion using a delayed-interference all-optical semiconductor gate assisted by nonlinear polarization rotation," submitted to Opt. Comm., Elsevier, the Netherlands, August 2008.
11. Jun Sakaguchi, "200-Gb/s waveform analysis of ultrafast all-optical semiconductor gates towards low-power consumption operation," PhD thesis (in English), Univ. Electro-Communications, June 2008.
12. Martin T. Hill, Harmen J.S. Dorren, Tjibbe de Vries, Xaveer J.M. Leijtens, Jan H. den Besten, Barry Smalbrugge, Yok-Siang. Oei, Hans Binsma, Giok-Djan Khoe, and Meint Smit, "A fast low-power optical memory based on coupled micro-ring lasers," Nature vol. 432, pp. 206-209, Nov. 2004.
13. Hitoshi Kawaguchi, Takeshi Mori, Yuuki Sato, and Yasuhiro Yamayoshi, "Optical buffer memory using polarization bistable VCSEL," CLEO/QELS 2006, May 21-26, 2006, Long beach, USA, paper no. CWG7.
14. Kiyoshi Asakawa, Yoshimasa Sugimoto, Yoshinori Watanabe, Nobuhiko Ozaki, Akio Mizutani, Yoshiaki Takata, Yoshinori Kitagawa, Hitoshi Ishikawa, Naoki Ikeda, Koichi Awazu, Xiaomin Wang, Akira Watanabe, Shigeru Nakamura, Shunsuke Ohkouchi, Kuon Inoue, Martin Kristensen, Ole Sigmund, Peter I. Borel, and Roel Baets, "Photonic crystal and quantum dot technologies for all-optical switch and logic devices," New J. Physics, vol. 8, p. 208, 2006.
15. Philip E. Ross, "Why CPU frequency stalled," the data, IEEE Spectrum, April 2008 issue, p. 52.
16. R. Suzuki, T. Ohira, J. Sakaguchi, and Y. Ueno, '40-GHz mode-locked pulse generation with a new scheme of SOA-based pulse generation,' CLEO/QELS 2006, May 21-26, 2006, Long beach, USA, paper no. CMG5.
17. R. Nakamoto, R. Suzuki, T. Ohira, J. Sakaguchi, and Y. Ueno, "160-GHz-class optical-clock circuit with semiconductor optical amplifiers,' AICT symposium, September 17-19, 2007, BUPT, Beijing, China, student session.
18. Ryoichi Nakamoto, Hiroyuki Takeuchi, Jun Sakaguchi, and Yoshiyasu Ueno, "1.55-um, mode-locked, single-longitudinal-mode, 10-GHz, 2-ps, ultra-short optical pulse train from our original semiconductor-based pulse-source scheme," Topical Conference on Nanophotonics (NANO), Optical Society of America, May 26-29, 2008, Southeast Univ., Nanjing, P.R. China, paper no. Nano-08-191.
19. Hiroyuki Takeuchi, Ryoichi Nakamoto, Jun Sakaguchi, Takashi Ohira, and Yoshiyasu Ueno, "Physical factors that define the preciseness required in our original, semiconductor-laser cavity scheme for generating 5-picosecond, 40-GHz, optical clock pulses," AICT symposium, October 7-9, 2008, ICU, Daejeon, Korea, student session.
20. Takehiro Nishida, Ryoichi Nakamoto, Jun Sakaguchi, Satoshi Shinada, Naoya Wada, and Yoshiyasu Ueno, "Experimental research of a 300-Gb/s-class, semiconductor-based all-optical gate which contains an optical-spectrum's amplitude-and-phase synthesizer," AICT symposium, October 7-9, 2008, ICU, Daejeon, Korea, student session.