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All-Optical Divided-Clock Extractor Using an Ultrafast All-Optical Symmetric-Mach-Zehnder-Type Semiconductor Switch Embedded in an Optical Loop

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We propose an ultrafast all-optical divided-clock extractor in which an all-optical symmetric-Mach-Zehnder (SMZ)-type semiconductor switch and a passive energy-distribution Mach-Zehnder interferometer are embedded in an optical loop. The extractor generates ultrashort optical clock pulses at a divided clock frequency (f_0/N, $N = 1, 2, 3, 4, \ldots$) from optical-time-division-multiplexed (OTDM) input packets at a bit frequency, f_0. Numerical results reveal that the phase of 40 GHz 1 ps clock pulses locks within 20 ns (which corresponds to 3,000 bits of a 160 Gb/s signal) to that of the 160 Gb/s pseudorandomly encoded input pulses.

KEYWORDS: clock extraction, divided clock, semiconductor, Mach-Zehnder, all-optical, ultrafast, loop, packet network, numerical, pseudorandom

As wavelength-division-multiplexing (WDM) network technology matures, ultrafast optical-time-division-multiplexed (OTDM) packet networks[1–3] are attracting attention because they offer more flexible and efficient communication than WDM networks. The ongoing progress in ultrafast all-optical semiconductor switches is steadily opening the way to OTDM signal rates of 160 Gb/s and even higher.[4–10] In such an ultrafast OTDM packet network, the clock must be extracted almost instantaneously from the ultrahigh-bit-rate packets. Conventional phase-locked-loop-type clock extractors require too much time with respect to the packet lengths.

Recently, Lee *et al*. have shown that an all-optical switch embedded in an optical loop structure functions as an all-optical clock extractor.[11] Using the all-optical switch proposed in ref. 12, they extracted 10 GHz optical clocks from 10 Gb/s optical signals. However, they did not evaluate the locking speed of the extractor. Manning *et al*. have shown that an all-optical switch embedded differently in a loop functions as a clock divider.[13] Their device generated 20 GHz divided-clock pulses from 40 GHz clock pulses in approximately 100 μS, but obviously it is not capable of extracting a clock from a digital signal.

This paper proposes an all-optical divided-clock extractor in which an ultrafast symmetric-Mach-Zehnder (SMZ)-type switch (as in refs. 4–10) and a passive energy-distribution Mach-Zehnder interferometer (ED-MZI) are embedded in a loop. The active part of this extractor (the SMZ switch) can all-optically form ultrashort (1.5 ps), ultrahigh-frequency (168 GHz) pulses using low-energy (1 fJ) input signal pulses.[10] The extraction response, which is determined by a product of the loop circulation time (*e.g.*, 400 ps for an 8 cm silica loop) and the required number of optical pulse circulations, can be very fast. The loop structure can be integrated on a small-size planar lightwave circuit, as in ref. 9. We present the numerical results of the divided clock extraction. The calculation is based on our all-optical switch simulator (see Appendix), which has successfully reproduced our experimental results of 7 ps 42 GHz switching[14] and 1.5 ps 168 GHz switching.[10]

The SMZ-loop-type divided-clock extractor is shown schematically in Fig. 1. It consists of a delayed-interference signal-wavelength converter (DISC),[14,15] the ED-MZI, a continuous-wave (CW) laser source, and polarization controlling components. The DISC consists of a semiconductor optical amplifier (SOA), a passive Mach-Zehnder interferometer, and a band-pass wavelength filter. The SOA is biased with a direct current for carrier injection (we do not need to electrically modulate the SOA). The ultrafast response of the DISC, which functions as an all-optical gate for a CW light, is assured by a mechanism similar to that in the SMZ switch. In the extractor, the delay time between the propagation times of the two split CW components in the DISC's MZI determines the clock pulse width to be generated. The relative phase between the DISC's MZI arms is optimized by using a phase shifter in one arm, as in ref. 14. The ED-MZI's frequency is designed to be equal to the clock frequency; that is, the ED-MZI's delay time is designed to be equal to the average clock pulse distance. Phase adjustment between the ED-MZI's arms is not needed. The loop frequency is adjusted to coincide with one of the harmonics of the clock frequency.

First, we examined this loop device without any input signal. A specific clock pulse sequence can keep circulating around the loop without changing its shape as follows. A

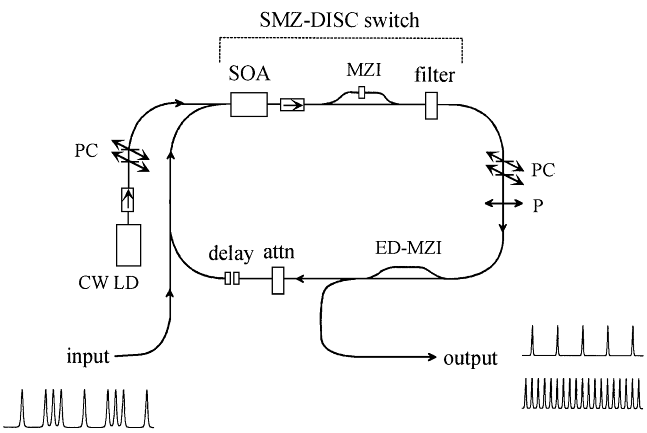

Fig. 1. All-optical divided-clock extractor. SOA: semiconductor optical amplifier, MZI: Mach-Zehnder interferometer, ED-MZI: energy-distribution MZI, PC: polarization controller, P: polarizer, attn: attenuator.

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pulse (A1) entering the SMZ-DISC switch with the orthogonally polarized CW light at time t_1 controls the switch and then the switch gates the CW light so that the CW light passes through the switch from t_1 through $t_1 + \Delta t$ only (Δt is the DISC MZI's delay time). Thus, a new pulse (B1) whose width is approximately equal to Δt is formed at the switch output. Because the new pulse is composed of the CW light, the new pulse's polarization is orthogonal to that of the original pulse. The new pulse passes through a band-pass filter and polarizer. In the meantime, the original pulse A1 is amplified by the SOA and split into two consecutive pulses after the DISC's MZI. These two original pulses pass through the filter but are blocked by the crosspolarizer. The crosspolarizer also prohibits the loop from lasing. The band-pass filter blocks most of the spontaneous emission from the SOA. When the new B1 pulse reaches the ED-MZI, the ED-MZI splits the B1 pulse into two pulses, B1 and B1′. Because the ED-MZI's delay time is preset to the clock pulse distance, the B1′ pulse is superimposed on the next new pulse, B2. These new pulses return to the DISC. Thus, the clock pulses, whose width and distance are determined by the DISC's MZI and the ED-MZI respectively, keep circulating around the loop.

Numerical calculation showed that any digitally coded pulse sequence changes to a clock pulse sequence after it circulates around the loop a few ten times. The calculated waveforms in Fig. 2 show one example of such transition. Here, a digitally coded 64-bit-long 160 GHz 1.5 ps pulse sequence [Fig. 2(a)] was assumed to enter the loop. The loop structure was assumed to be integrated on a silica lightwave circuit and the loop length was set to 8 cm so that the first bit of the circulating sequence followed the last bit of the sequence. In other words, the loop frequency was 160 GHz/64 = 2.5 GHz. As the pulse sequence circulated in this loop, the 160 GHz ED-MZI uniformly distributed the pulse energy every 6.25 ps [Figs. 2(b) and 2(c)]. After 32 circulations, the pulse sequence completely changed to a 160 GHz clock pulse sequence. In the meantime, the DISC, with a gating window width of 1.0 ps, compressed the pulse width to 0.97 ps.

The calculated waveforms in Fig. 3 show another example of such a transition. The 160 GHz ED-MZI was replaced with a 40 GHz ED-MZI, which distributed the pulse energies every 25 ps. As a result, only the 40 GHz pulse components out of the 160 GHz pulse seuqence survived, while the other components were removed [Figs. 3(b)–3(d)]. This removal originates not only from the ED-MZI but also from the sinusoidal transfer function of the DISC (when the DISC receives a weak A1 pulse, it outputs an even weaker new B1 pulse due to this function). After 16 circulations, a uniform 40 GHz clock pulse sequence was formed [Fig. 3(d)].

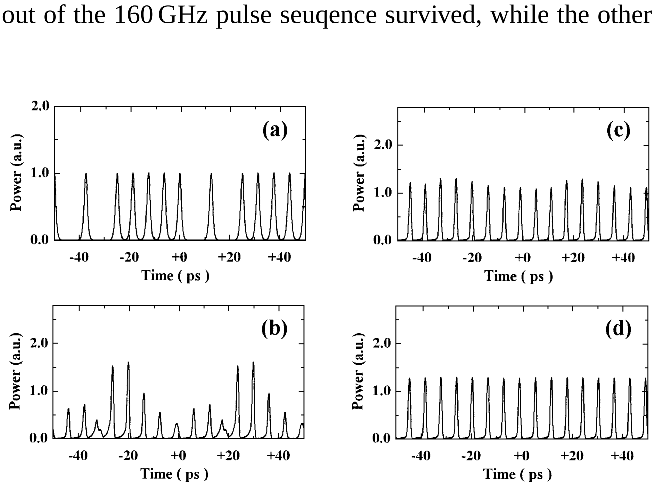

Fig. 2. Calculated waveforms of pulses circulating around the loop. The ED-MZI's delay time was set to 6.25 ps (160 GHz^{-1}). (a) Middle part of the initial 64-bit-long 160 Gb/s pulse sequence, (b) after four circulations, (c) after 16 circulations, (d) after 32 circulations.

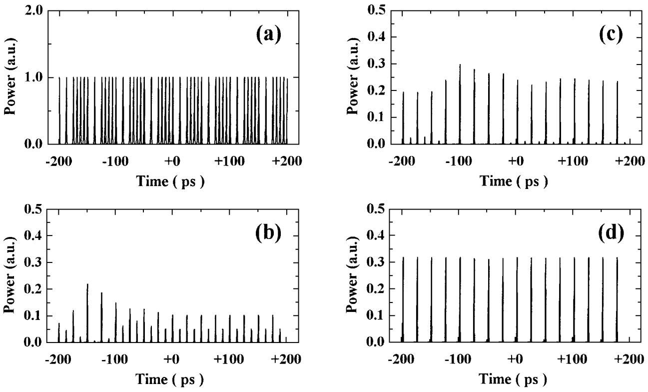

Fig. 3. Calculated waveforms of pulses circulating around the loop. The ED-MZI's delay time was set to 25 ps (40 GHz^{-1}). (a) Entire waveform of the initial 64-bit-long 160 Gb/s pulse sequence, (b) after four circulations, (c) after 8 circulations, (d) after 16 circulations.

When the loop received appropriately weak digitally coded signal pulses from the input port, the phase of the clock pulse sequence inside the loop quickly locked to the input signal. Figure 4 shows a calculated example of 40 GHz clock pulses being extracted from pseudorandomly coded 160 Gb/s signal pulses. The pseudorandom word length was set to 2^{15}–1 and the mark ratio was set to 1/2. For the SOA, a carrier lifetime of 60 ps, a pulse gain saturation energy of 180 fJ, an unsaturated gain of 28 dB, and an injection current of 300 mA were assumed.[14] The excess loss of the loop was assumed to be 5 dB. The average power of the input signal pulses, that of the circulating clock pulses, and the CW light power were 20, 288, and 90 μW, respectively, at the SOA input.

The phase of the extracted clock [solid curve in Fig. 4(a)] locked to the input phase [dashed curve] within 50 circulations, which takes 20 ns. The locking time of 20 ns corresponds to 3,000 bits of 160 Gb/s signal. As shown in Fig. 4(a), we also intentionally gave the input phase a jump and drift. The phase of the extracted clock continued to track these input phase fluctuations. The phase's response time at the phase jump was also approximately 20 ns. When the clock pulses locked to the input signal, the optical phase of each pulse was in-phase to that of the incoming input signal pulses at the SOA input (the input signal pulses interfere constructively with the circulating clock pulses). Results similar to Fig. 4 were obtained for a relative input frequency range of $\pm 5 \times 10^{-5}$.

Figures 4(b) and 4(c), respectively, show a typical waveform and a Fourier-transformed RF spectrum of the extracted 40 GHz clock pulses (the input signal pulses almost completely disappeared after the DISC, because of the sinusoidal transfer function of the DISC). The clock pulses were as narrow (0.8 ps) as the pulses in Figs. 2(d) and 3(d). The slight nonuniformity of the peak heights in Fig. 4(b), which originated from the 10 GHz subharmonic components seen in Fig. 4(c), was within ± 0.64 dB.

We suspect that the 10 GHz components remained because this frequency is a harmonic of the loop frequency (2.5 GHz)

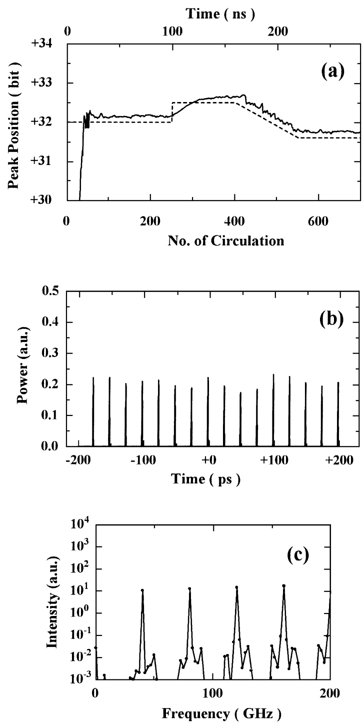

Fig. 4. Calculated results for the all-optically extracted 40 GHz divided-clock pulses. (a) Phase of the extracted 40 GHz clock (solid curve) in comparison with that of the 160 Gb/s input signal (dashed curve), where the input phase was caused to jump and drift, (b) clock waveform after 700 circulations, (c) RF spectrum of the clock pulses.

as well as a subharmonic of the clock frequency. We believe that such subharmonic components will be further suppressed by appropriately designing the loop frequency. When the ratio of the clock frequency to the loop frequency is an elementary number (for example, when the ratios between the input, the clock, and the loop frequencies are 160 GHz : 40 GHz : 2.353 GHz = 68 : 17 : 1), no harmonic of the loop frequency coincides with a subharmonic of the clock. Such a loop design will suppress the subharmonics and improve the clock's peak uniformity.

In summary, we proposed an ultrafast all-optical SMZ-loop-type divided-clock extractor that allows only a specific clock pulse sequence to circulate around the loop. The clock frequency and its pulse width are optically determined by the delay-time designs of two passive MZIs inside the loop. When the extractor receives signal pulses whose frequency is close to the harmonics of the predetermined clock frequency, the phase of the clock pulses quickly locks to that of the input signal. Based on numerical calculation, we demonstrated 40 GHz divided-clock extraction from ultrafast 160 Gb/s signal pulses. The clock phase locked to the input phase within 20 ns. The response time, locking range, and peak uniformity will be improved by further optimizing the device design.

Acknowledgements

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Appendix: Basic Equations and Material Parameters Used in the Numerical Calculation

In calculating the detailed ultrafast reactions of the all-optical DISC, we assumed that the nonlinear refractive index change is proportional to the carrier density change and the material gain is proportional to the carrier density.[14] Accordingly, the nonlinear phase shift $\Delta\Phi_{\mathrm{NL}}(t)$ given to the co-propagating CW light in the SOA is written as

$$\Delta\Phi_{\mathrm{NL}}(t) = k_0 \cdot dn_{\mathrm{r}}/dn_{\mathrm{c}} \cdot \lfloor n_{\mathrm{c}}^0 - n_{\mathrm{c}}(t) \rfloor \cdot \Gamma L. \qquad \text{(A·1)}$$

It should be noted here that we can use a longitudinally averaged carrier density $n_{\mathrm{c}}(t)$ instead of $n_{\mathrm{c}}(t,z)$ (z: distance along the cavity) when we assume the above-mentioned proportionalities, in a manner similar to the modeling of pulse gain saturation.[16] The carrier density $n_{\mathrm{c}}(t)$ is depleted at the arrival of each input pulse $E_{\mathrm{IN}}(t)$ as

$$\frac{d}{dt} n_{\mathrm{c}}(t) = \frac{I_{\mathrm{op}}}{qV} - \frac{n_{\mathrm{c}}(t)}{\tau_{\mathrm{c}}} - \frac{1}{V} \cdot [G_1[n_{\mathrm{c}}(t)] - 1] \cdot \frac{|E_{\mathrm{IN}}(t)|^2}{\hbar\omega}. \qquad \text{(A·2)}$$

The temporal gains G_1 and G_2 for the pulse and the CW component, respectively, are also modulated as

$$G_j(t) \equiv \exp[dg^j/dn_{\mathrm{c}} \cdot n_{\mathrm{c}}(t) \cdot \Gamma L], \quad j = 1, 2, \qquad \text{(A·3)}$$

where $dn_{\mathrm{r}}/dn_{\mathrm{c}}$, dg/dn_{c}, and τ_{c} are the nonlinear refractive index change, the differential gain coefficient, and the carrier lifetime of the SOA semiconductor. Γ, L, and V are the optical confinement factor, the length, and the volume of the SOA active layer. I_{op} is the current injected into the SOA.

The loop circulations of a 64-bit-long pulse waveform were calculated iteratively. The waveform was expressed by a double-precision complex vector with $2^{15} = 32,768$ elements. We numerically confirmed that the time resolution of $400\,\mathrm{ps}/2^{15} = 12\,\mathrm{fs}$ was sufficient in this work.