Theoretical models of the SOA-based SMZ-type optical-3R gates

Yoshiyasu Ueno, Masashi Toyoda, and Rei Suzuki

University of Electro-Communications, Chofugaoka, Chofu, Tokyo 182-8585, Japan, y.ueno@ieee.org

Abstract: We modeled the PDSMZ-type (UNI-type) 3R scheme and studied its available degree of amplitude-noise suppression in both '1' and '0' signals and possible waveform distortion. For evaluating the noise distribution, bit-error rates were calculated to below 1×10^{-6}.

1. Introduction

After optical-3R gating with 80-Gb/s-class pseudorandom signals has experimentally been achieved [1, 2] with an SOA-based polarization-discriminating symmetric-Mach-Zehnder (PDSMZ) gate (the PDSMZ gate structure [3] is sometimes called 'UNI'), its 3R capabilities has more practically been demonstrated in recirculating-loop, ultralong-haul transmission experiments with 40-Gb/s RZ and CS-RZ signals [4-7]. Potential applications of such SOA-based interferometric 3R gates include burst- and packet-mode network systems and optical buffer memories because of their low-power consumption and compactness after integration [8].

From theoretical modeling's viewpoints, however, the SOA-based SMZ-type gates in the 3R-gating scheme have not been modeled as clearly as those in the optical demultiplexing scheme [9, 10]. This is because those in the 3R-gating scheme are driven by pseudorandom RZ signals in contrast to those in the optical demultiplexing scheme are driven by divided clock pulses.

In this work, we report the latest results from our theoretical design models that we have been building since 2002 [11, 12].

2. The PDSMZ-type optical-3R gate scheme, and its theoretical model

The PDSMZ-type optical-3R gate scheme (Fig. 1) that has been used in the previous 3R-transmission experiments [4-7] was assumed in this work. The two cascaded PDSMZ gate structures in this 3R gate scheme were assumed to be identical to each other and be identical to the structure in Refs. [1] and [2]. The first PDSMZ gate that is receiving the input data pulses all-optically encodes the input clock pulses. At the output of the first PDSMZ gate, encoded data pulses are newly generated. The digital logic of the newly encoded data pulses can be either inverted or non-inverted, in general. The second PDSMZ gate that is receiving the newly encoded data pulses all-optically encodes the input clock pulses, once again. At the output of the second PDSMZ gate, the twice-encoded data pulses are generated whose digital logic is generally non-inverted.

The input data pulses in the theoretical model calculation were generated as,

$$E_{data}(t) = \sum_{m}(C_m \cdot E_m^1 + E_m^0)\cdot \mathrm{sech}(\frac{t - m\times T_0}{T_w}),\ \mathrm{m} = 1, 2, ..., N_b, \qquad (1)$$

where T_0 is the bit distance in time. The random binary sequence C_m (= 0 or 1) was generated with a pseudorandom binary number generator whose pattern length was set to 2^{31}-1. The random amplitude noise in the input data pulses was modeled, as follows. Analogue pseudorandom numbers in the normal distribution (pattern length= $2^{32} = 4\times10^9$) were generated independently from the digital random numbers and were superimposed separately on 1-bit amplitude E_m^1 and 0-bit amplitude E_m^0. The standard deviation of E_m^0 was set to a half that of E_m^1. For calculating the bit error rate (BER) at the output of the 3R regenerator, three million bits of input data pulses [i.e. N_b= 3,000,000] were repeatedly generated.

The carrier density n_c in the respective SOA was assumed to be instantaneously depleted by both data pulses and clock pulses, and then be recovered by the injection current with only one time constant τ_c. The rate equation that governs this ultrafast carrier-density oscillation was simply described as,

$$\frac{d}{dt}n_c(t) = \frac{I_{op}}{qV} - \frac{n_c(t)}{\tau_c} - \frac{1}{V}\cdot\left(G\{n_c(t)\} - 1\right)\cdot\frac{\left|E_{data}(t)\right|^2 + \left|E_{clock}^1(t)\right|^2 + \left|E_{clock}^2(t)\right|^2}{\hbar\omega}, \qquad (2)$$

in a manner similar to that in Refs [10]-[13]. The E_{clock}^1 and E_{clock}^2 are the non-delayed and Δt-delayed clock pulses at the input of each

SOA, respectively. The gain G and the optical nonlinearity coefficient of the SOAs were assumed to be insensitive to the input polarization and wavelengths.

Regarding the gating conditions (i.e. the input pulses' widths, the input pulses' energies, the delay time Δt, and the input data timing with respect to the clock), we systematically optimized each condition to the respective value in Table 1 so that the best regenerated eye diagrams were observed. (We have also paid attention to the previously reported conditions in Refs. [5] and [6].)

It should be noted that the optimum delay time Δt in this work was 61.7% of the bit distance. The bit logic after the first PDSMZ gate was inverted. The width of the input clock pulses was adjusted to be narrower than the input data pulses, and consequently the width of the encoded clock pulses was narrower that the input data pulses. We adjusted the width of the encoded clock pulses to that of the input data pulses by narrowing the spectral width of the two BPFs to 0.80 nm.

3. Available degree of amplitude-noise reduction after the two-cascaded 3R gate scheme

First, Fig. 2 shows calculated eye diagrams and BERs with using 42-Gb/s pseudorandom data pulses. At the output of the two-cascaded PDSMZ gates [Figs. 2(c) and 2(d)], the amplitude noise in the 1-bit pulses was remarkably suppressed in comparison with that at the input of the first PDSMZ gate. The amplitude noise in the 0-bit pulses was also suppressed. As a result, the range of the decision threshold that suppressed the bit error rate to below 10^{-6} was significantly expanded after this 3R regeneration [Fig. 2(f)]. The slope shape of the 'noise' distribution after the 3R gate clearly differed from that of the standard amplifiers. (As a consequence of this shape of noise distribution, the standard Q-factor may not be a good measure for evaluating this type of regeneration systems.)

For reference, Figs. 3(a) and 3(b) show calculated waveforms of the '100'-encoded clock pulses and the carrier-density oscillation under these optimum gating conditions. The so-called time-differential interference in Fig. 2 occurred as a consequence of a nonlinear optical phase shift of 0.36π induced by the carrier-density oscillation in Fig. 3(b), according to our calculation.

Second, we studied how this regenerator would tolerate to each of the gating conditions and what kinds of distortion and/or pattern-induced noise would outside the tolerance range, as follows. (1) When we broadened the width of the clock pulses from 3.0 ps to 5.0 ps, for example, several transient leakage components were observed in the '100'-encoded waveform [Fig. 3(c)]. (2) When we weakened the input clock power, another type of leakage components was observed [Fig. 3(d)]. (3) When we changed the width of the input data pulses in the range of 6-9 ps in contrast, the distortion in the waveform and eye diagram was relatively small. (4) We also investigated how the regenerator tolerates to the input timing of the data pulses.

4. Conclusion

We studied available degree of amplitude-noise suppression capability and possible waveform distortion outside the tolerance ranges, after building a theoretical design model of the cascaded-PDSMZ optical-3R scheme. The degree of noise suppression was evaluated by calculating the bit error rates to below 1×10^{-6}, for the first time to our knowledge. These modeling techniques will be useful for designing all kinds of ultrafast SOA-based interferometric gates and for supporting experimental research activities with limited monitoring equipments.

References: [1] A. E. Kelly, et al.., Electron. Lett. **35** (1999) 1477, [2] Y. Ueno, et al., IEEE PTL **13** (2001) 469, [3] K. Tajima, et al., Appl. Phys. Lett. **67** (1995) 3709, [4] H.J. Thiele, et al., Electron. Lett. **35** (1999) 230, [5] M. Tsurusawa, et al., OFC 2003, ThX3, [6] Y. Hashimoto, et al., ECOC 2003, Mo 4.3.3, [7] R. Inohara, et al., ECOC 2004, We 2.5.3, [8] J. Sarathy, OFC 2005, OThE1, [9] S. Nakamura, et al., IEEE PTL **12** (2000) 425, [10] Y. Ueno, et al., IEICE Trans. Electron. **E86-C** (2003) 731, [11] Y. Ueno, Opt. Comm. **229** (2004) 253, [12] R. Suzuki, et al., OECC 2004, 13E2-1, [13] Y. Ueno, et al., J. Opt. Soc. Am. B19 (2002) 2573.

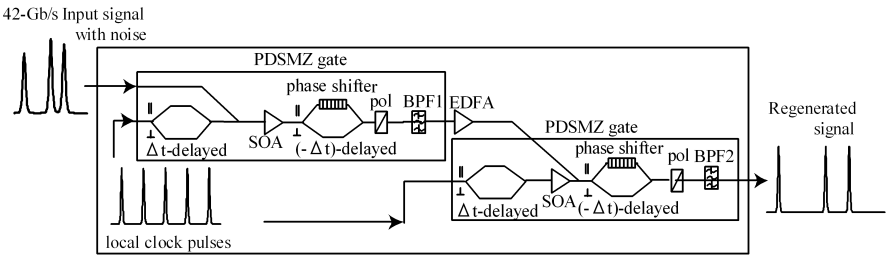

Fig. 1: The two-cascaded PDSMZ-type 3R gate scheme [5-7]

Table 1: The parameters used in this work.
width: full width at half maximum.

Description	Value
Input data's pulse width	6.0 ps @42 Gb/s
Input data's pulse energy	100 fJ
Input clock's pulse width	3.0 ps
Input clock's pulse energy	400 fJ
Unsaturated gain of SOAs, G_0	28 dB
Gain saturation energy of SOAs, P_{sat}	180 fJ
Carrier lifetime of SOAs, τ_c	50 ps
Nominal injection current, I_{op}	150 mA
Enhanced current injection to the SOAs	440 mA
Injection enhancement factor	2.9
Interferometer delay time, Δt	14.7 ps (61.7%)
Interferometer phase bias, $\Delta\Phi_b$	1.0π
Nonlinear phase shift, $\Delta\Phi_{NL}$	0.36π
Width of the bandpass filter	0.80 nm (Gaussian)
Regenerated data's pulse width	6.4 ps

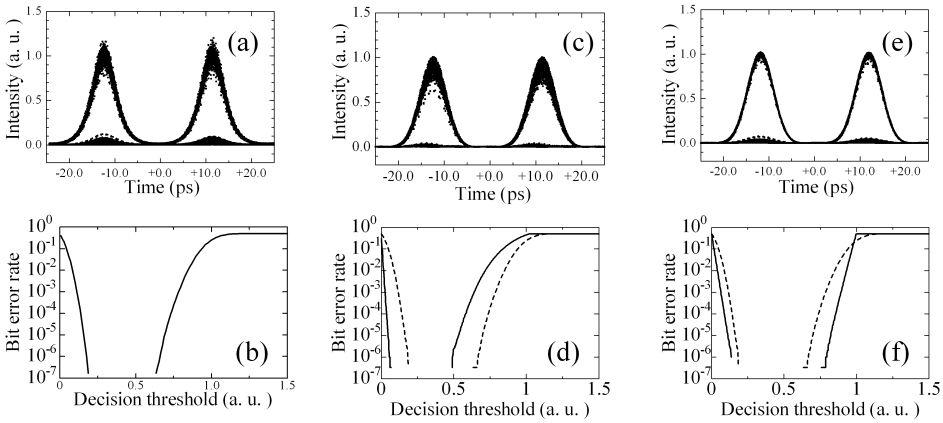

Fig. 2: Calculated eye diagrams and BERs with 42-Gb/s random data pulses
(a), (b): Input data pulses.
(c), (d): Logic-inverted data at the output of the first PDSMZ gate.
(e), (f): Regenerated, non-inverted data at the output of the two-cascaded PDSMZ gates.
Dashed curves in (d) and (f) indicate the BERs in (b), for comparison.

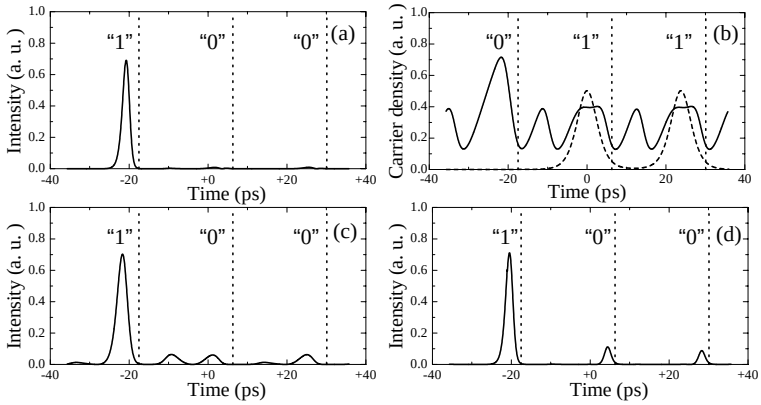

Fig. 3: Calculated 42-Gb/s waveforms
(a): Clock pulses after being encoded by 6.0-ps "001" data pulses (before broadened by the BPF).
(b): Carrier-density oscillation with the optimum conditions. Dashed curve: input data pulses "011".
(c): Encoded clock pulses where the input clock pulse's width was too broad (5.0 ps).
(d): Regenerated data waveform where the input clock pulse's power was too small.