Roadmap of ultrafast energy-saving optical semiconductor devices to Year 2025

--- <speed, energy, size> estimates of optical Micro Processor Unit ---

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Contents

[1] Total energy consumptions in ICT technology

[2] Recent trends of optical-data-processing devices <speed, energy, size>

[3] All-Optical gates: from principles to new potentials <speed, energy, size>

[4] Crude estimates about “optical MPU” (long-term research)
   (first time, too, to our knowledge)

Co-authors and Collaborations
Energy consumptions in ICT-related systems

Conventional Technol. (electronic MPU's)

Around 2005, Clk freq. reached 3 GHz.

Nano-materials inside MPU’s are nearly melt.

(37 years of Moore’s law, IEEE 2008)

In Data Centers of Google, Microsoft, etc.

Clk freq.: 3 GHz, with similar MPU’s

Heat-energy dissipation: 10 kW / sever rack

Data-center energy: 20 MW / data center

We need ultrafast & energy-saving Optical Transistors in future!

Ultrafast Optical Logic Lab., UEC
Electric-energy consumptions, 1970-2006

[1] Impacts of ICT energy consumptions

Primary energy supply, for electricity

Year


World

Japan

P.R. China

India

EU (15)

UK

USA

China

EU (15)

UK

USA

World

Primary Energy Supply for generating the annual total electricity supply in the country (EJ)

*1) Source: International Energy Agency (IEA), Paris,
Energy balances of OECD countries and non-OECD countries.

*2) 1 EJ = 1 × 10¹⁸ J.
Macro-scopic: Primary Energy Supplies (sum of electricity and non-electricity), 2006

[1] Impacts of ICT energy consumptions

**Primary Energy Supplies**

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<table>
<thead>
<tr>
<th>Country</th>
<th>Total Primary Energy Supply (EJ, 2006)</th>
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<tr>
<td>Japan</td>
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<td>China</td>
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<td>EU</td>
<td>80</td>
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<td>USA</td>
<td>70</td>
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**Ratios of energy for electricity**

```
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<th>Country</th>
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<th>for non-electricity</th>
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<tr>
<td>Japan</td>
<td>39%</td>
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<td>China</td>
<td>36%</td>
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<td>EU</td>
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<td>USA</td>
<td>43%</td>
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**GDP’s (2006)**

```
<table>
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<th>Country</th>
<th>GDP (x 10^11 USD, 2006)</th>
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<tr>
<td>Japan</td>
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<tr>
<td>China</td>
<td>6,000</td>
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<td>EU</td>
<td>8,000</td>
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<tr>
<td>USA</td>
<td>10,000</td>
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</table>
```

Data Centers in USA consuming 1.5% of all electricity (D. Miller, Stanford).

→ Not very large?? → 1.5% corresponds to **10 nuclear reactors!!**

→ We need energy-saving devices.
Micro-scopic: one origin of ICT-energy consumptions

Tr-number times Clk-freq. has evolved by a factor of $10^6 \times 10^4 = 10^{10}$ (in 40 years)

- **Tr number**: $10^6$
- **Clk freq.**: $10^4$

- **FLOPS speed has increased by $10^{10}$.**
- **MIPS speed has increased by $10^4$, only, without supported by Tr number.** (reasonable)
- **Already relying** on parallel-processing MPU's and software. many-folded parallel-structures are probably pushing-up electric-energy consumptions (and costs). [hard to quantitatively characterize now, though.]

**Tr • Clk Product**

Moore’s magic

Sources: FLOPS from measured results, MIPS from wikipedia.

**? for 2010-2050:** Increasing demands are FLOPS-type demands, or, MIPS-type demands ??

Y. Ueno, February 2010

Cray Jaguar, IBM Roadrunner
NEC-Sun Tsubame -> NEC Earth simulator ->

Peta

Crystalline Jaguar, IBM Roadrunner

Tera

Pentium Pro (1996)

Giga

80386 (1985)

Crystalline-1 ->

8086 (1978)

8086 (1985)

Core 2 Quad (2007)

Pen 4 (2002)

80386 (1985)


FLOPS

(MIPS)

no. of Trs. times clk freq. 10x every 4 yrs.
FLOPS 10x every 4 yrs.
Instructions per sec. 10x every 7 yrs.
to move from electronics to optics: its famous weakness

Latest degrees of integrations for optical-processing devices

Number of devices on one chip = 200 (Infinera, 2006)

→ evolving steadily, driven by industrial demands,
and approaching the number 2,300 in intel 4004 (1971).

source: 

All-Optical circuits w/ gates & memories

Optical data

Drive energy (electric dc-bias)
(2-1) Optical buffer memories (fundamental-research)

- **25 Gb/s, 1 pJ/bit, (30 μm)²**
  - M.T. Hill (Smit Gr., Eindhoven), planar, ring-laser.

- **40-100 Gb/s, 3 pJ/bit, (10 μm)²**
  - T. Katayama (Kawaguchi Gr.), 2009, Vertical, VCSEL.

- **40-160 Gb/s, L = few mm long**
  - E. Kehayas (Dorren Gr., Eindhoven), planar, coupled-gates.

In bulk or MQW semiconductors, photon-electron interactions are used.

- **Photonic-crystal gate**
  - (FESTA, U. Tsukuba, AIST)

K. Asakawa et al., J. of Phys. 2006

Ultrafast Optical Logic Lab., UEC
(2-2) All-optical gates (for practical signal-conversion, 2R/3R, demux, etc.)

SMZ-DISC scheme, with non-linear cross-phase modulation XPM

Gate, 2000年

168Gb/s, 2 pJ/bit, L= 1mm
S. Nakamura, Ueno, Tajima (NEC), wavelength-conversion

Gate, 2006年

320Gb/s, 2.5 pJ/bit, L= 1mm
Y. Liu (Eindhoven), wavelength-conv.

Gate, 2009年

640Gb/s
T. Hirooka (Tohoku U. & NEC), Demux.
Latest optical gates and memories

Optical-data-processing “gates and memories” <speed, energy, size>

(2-2) All-optical gate (fundamental-research in our univ. UEC, Tokyo)

SMZ-DISC scheme (XPM) in our group

Converter, XOR, AND, 2R/3R, etc.

Flip-Flop (Eindhoven, Tsukuba)

Clock oscillator (UEC)

Gate, 2008

Distance in air, z (mm)

-20  -10  0  +10  +20

Gated waveform, 1540 nm

200Gb/s, 3 pJ/bit, L ≅ 1mm


Oscillator, 2005-2008

Wavelength (nm)

1552 1550 1548 1546

Intensity (dBm/nm)

-60  -40  -20  0

550 GHz

193.0 193.5 194.0

Optical frequency (THz)

(160G-class)

Δ2ps/40GHz optical clock oscillator

200-Gb/s gated waveforms, 
_in the middle_ of our experimental studies


[2] Latest optical gates and memories

Data-pattern-induced amplitude noise

- badly gated (too slow)
- (accelerated) better

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Ultrafast Optical Logic Lab., UEC
COE-research: DISC-loop-type mode-locked pulse source

2-ps, 40-GHz pulse and comb generation, 2005-2006


Auto-correlation trace

Optical-frequency-comb spectrum

measured t-f product, \( \Delta t \Delta f = 0.53 \)
(1.2 times that of a Gaussian pulse)

Proof of principle (1), threshold behavior

Proof of principle (2), linearly controlled pulse widths

solid curve: 10 GHz
dashed curve: 40 GHz

Ultrafast Optical Logic Lab., UEC
fundamental research of “gates”

Flip-Flop (Eindhoven, Tsukuba)

Clock oscillator

single-longitudinal-mode mode-locking, 2008
(with using high-Q etalon filter designed by JAE Japan)

precise, only-one-mode lasing out of Δ10-MHz-spacing modes.
(Nakamoto, et al. OSA-NANO 2008)

Original features of this scheme of ours:

- 500-GHz-BW comb, low power consumption, integration possibility (presently)
- precise optical frequency, \( f_{\text{opt}} \) (locked to external DFB source, \( f_{\text{opt}} \))
- precise repetition frequency, \( f_R \) (locked to dielectric etalon’s FSR, \( f_R \))
- precise comb envelope shape, \( f_{\text{BW}} \) (locked to dielectric MZI delay time, \( \Delta t \))
status of Modeling-research (optical gates)

Subject: about the useful correlation between sensitive dependences of waveform and spectrum, on the optical phase bias, $\Delta \Phi_B$

Conclusion:
we’ll be able to feedback-control the 160-Gb/s Demux by monitoring the “supervisory” spectrum

Ultrafast Optical Logic Lab., UEC
To solve this, within DISC scheme, we need a kind of imbalance factor between the two interferometer arms.
[3] Physics and potentials, of all-optical gates  <speed, energy, size>

Quote: “All-optical semiconductor gate seems too complicated”
--- Prof. Guifang LI, CREOL/UCF, USA.

Inversion-population semiconductors (SOA’s)

- nonlinear dependences → unsaturated gain $G_0$, gain-saturation energy $P_{\text{sat}}$, optical 3R/2R.

- linear dependences (many ways) → in gate speed, energy, size.

Ueno et al., JOSAB 2002

“not so complicated !!”

Linear dependence

Ueno et al., JOSAB 2002

"not so complicated !!"
Physics: Refractive-index modulations, etc., due to excited-electron-hole-density modulations

K. Tajima (NEC 1993)  
J. Sokoloff (Princeton 1993)

Step-wise processes in generating optical outputs, Z and X'.

1. Stimulated amplification of optical inputs X and Y.
   - (2) electron density is modulated (in materials).
   - (3) refractive index is modulated (in materials).
     Material's rise time = 100 fs (fall time is slower).
   - (4) optical phase is modulated (in optical signal X or Y).
   - (5) modulated lights are coherently combined, before gate’s output.
   - (6) new optical outputs, Z and X' are generated.

Drive energy = dc-electron-injection energy (dc-bias current)
Speed of gates

[3] All-optical gates/speed

faster than material-relax. speed, after optically accelerating the material

Origin: R. Manning (BT), EL 1994

- For gates, this acceleration is equivalent to “faster materials”
- Energy consumption is equivalent to them, as well.

\[
\frac{\text{d} n_c}{\text{d} t} = \frac{I_{op}}{qV} \left( \frac{G[n_c] - 1}{V} \right) \times \frac{|E_{accel}(t)| + |E_{data}(t)|^2}{h\omega}
\]

experimentally recognized.
(Sakaguchi, et al., Opt. Express 2007)
Speed of gates, more simply

Ueno et al., JOSAB 2002

Principle of acceleration (in SOA)

- $|\text{excited}\rangle$ (quasi-fermionic)
- Continuous pump (efficient)
- $|\text{g}\rangle$ (transparent-state)

Relax. due to stimulated-emission (with seed cw or clock) = optical acceleration

Material level: nonlinear dependence

Linear dependences after optical acceleration

Gate performance: linear dependences show-up.

Energy per bit $\Phi$ speed (due to Joule loss)
Helpful for designs and experiments

Several other linearities:
- Optical phase mod.
- Electron density mod.
- Optical phase mod. $\Delta$ interaction length
- Optical phase mod. $\Delta$ electron-photon overlap

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Speed of gates \(\rightarrow\) numbers at operating point (200Gb/s)

**Principle of gate = electron-pump**

- Optical input (30fJ/bit)
- Acceleration (cw, 100 fJ/bit)

- Electrons
- Holes

- Optical pulses
- Amplified pulses

- SOA


- 168G input data
- 168G output data

![Graphs of 168G input and output data with signal levels and delay values.](image)

- Material \(> 60\)ps \(\rightarrow\) gate recovery \(< 6\)ps

- Electron consumption = \(1 \times 10^7\) electrons/bit
- Electric-energy consumption = 3 pJ/bit

Nearly-regardless of material's speed (in this regime)

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[3] All-optical gates/ speed

Energy-efficiency of gates $\rightarrow$ new potentials in near-future (--2025)

Other institutes: packet-routing, buffer memories, integrated 2R-subsystem.

Our group (UEC): following directions (for energy-saving)
- blue-shift filter $\rightarrow$ Nielsen et al., Opt. Express 2006
- spectral-synthesis scheme $\rightarrow$ going-on (Nishida et al., IEEE-LEOS 2009)
  (UEC-NICT collaboration, FY2007-)
- (non-deg. $\rightarrow$) degenerate-scheme $\rightarrow$ going-on
  [free from polarization-insensitivity requirements]

not yet started but, from near-future
- QW-band-engineering, for enhancing refractive-index mod.
  (e.g., ACQW)

further
- efficient pump (optical)
- low-dim., surface plasmon, nano-photo

300 pJ/bit
30 pJ/bit (previously)

3 pJ/bit (present)

0.3 pJ/bit
(near future)

100-fJ to 30-fJ
(far future)
Size of gates → interaction L, new potentials in near-future (--2025)

dc-electron pump (at present)

energy supply of 3 pJ/bit, that is, $1 \times 10^7$/bit of electrons, in interaction length= 1 mm

Volume density of excited electrons $> 2 \times 10^{18}$ cm$^{-3}$?

experimentally: stock= relatively dilute $(2 \times 10^{17}$ cm$^{-3}$)!

Sakaguchi et al., Optics Express 2007 through present

→ flow (modulation)= less efficient (at present)

one of new potentials

10-times more electron density $(2 \times 10^{18}$ cm$^{-3}$),

→ 10-times shorter gate length $(L= 100$ μm$)$

(Hetero-barrier energy seems not enough, at present)
volume density of excited electrons (cm$^{-3}$)

- **Metals**
  - Al, Au, Ag, Cu
  - Volume density: $1 \times 10^{22}$
- **Plasmonics**
  - (very lossy)
- **Spintronics**
  - “half-metal”
  - Mn: GaAs
- **Semi-conductors**
  -  (un-doped, intrinsic)
  - Volume density: $1 \times 10^{16}$
- **Semi-metals**
  - Volume density: $1 \times 10^{20}$
- **Ill-V in all-optical gates (presently)**
  - Super-dense electrons in Ill-V, $10^{18} \sim 10^{19}$
  - Unexpectedly dilute, $2 \times 10^{17}$

**References**

- [3] All-optical gates/ size
- [24] Ultrafast Optical Logic Lab., UEC

**Background levels**

Super-high-density electron-confinement, with new hetero-barrier systems

\[ E_g = k_B T \times 35 \]

**Presently**
- 1.55 \( \mu m \) InGaAs/InP (550 meV)
- 1.31 \( \mu m \) InGaAsP/InP (400 meV)
- 1.31 \( \mu m \) AlGaInAs/InP (750 meV)

**Future**
- 0.87 \( \mu m \) GaAs/AlGaInP (920 meV)
- 0.98 \( \mu m \) InGaAs/AlGaAs (760 meV)
- 920 meV hetero-barrier (= \( k_B T \times 35 \))
### Optical micro-processor, near Year 2025

**near-future**: speed=300G, energy=0.3pJ/bit, size(interaction)= 100μm

<table>
<thead>
<tr>
<th>Specification</th>
<th>Electronic</th>
<th>Optical processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Demo Year</strong></td>
<td>Year 1971</td>
<td>Year 2000-2010</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>500 kb/s</td>
<td>200-300 Gb/s</td>
</tr>
<tr>
<td><strong>Energy (per bit)</strong></td>
<td>3-10 pJ/bit/gate</td>
<td>0.3 pJ/bit/gate</td>
</tr>
<tr>
<td><strong>Size (per gate)</strong></td>
<td>70×70 μm²</td>
<td>1,000×3,000 μm²</td>
</tr>
<tr>
<td><strong>Number of gates (per chip)</strong></td>
<td>2,300 transistors</td>
<td>several</td>
</tr>
<tr>
<td><strong>Energy dissipation (per chip)</strong></td>
<td></td>
<td>2,300 gates</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(6 chips on 3-inch wafer)</td>
</tr>
</tbody>
</table>
Earlier statements:
- already relying on parallel-processing structures, which are probably pushing-up their electric-energy consumptions.
- Increasing demands in 2010-2050 are FLOPS-type demands or MIPS-type demands??

Y. Ueno, February 2010

Out: FLOPSは市販PC計測結果、MIPSはwikipedia資料。

Cray Jaguar, IBM Roadrunner
NEC-Sun Tsubame -> NEC Earth simulator ->

Cray-1 ->
Relative performance of optical-processor 4004

Optical processor (estim.)
alternative to Moore’s law

number-integration

Cray Jaguar, IBM Roadrunner
NEC-Sun Tsubame ->
NEC Earth simulator ->

Tr • Clk • Product

Zetta
Exa
Peta
Tera
Giga

intel 4004 (1971)
Core 2 Quad (2007)

(M)IPS matches to Core 2 quad (2007).
FLOPS will be weak.
Power consumption: 200 Watts

Y. Ueno, February 2010

_outcome:
FLOPS is measured results of PC.
MIPS is wikipedia data.

Ultrafast Optical Logic Lab., UEC
## Sample Spec. Numbers of Optical-80386

<table>
<thead>
<tr>
<th></th>
<th>e-80386 (32-bit)</th>
<th>e-Core2_quad (32-bit/64-bit)</th>
<th>Optical 80386 (32-bit)</th>
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<tbody>
<tr>
<td></td>
<td>1985</td>
<td>2007</td>
<td>2025</td>
</tr>
<tr>
<td><strong>Unit</strong></td>
<td><strong>Hz</strong></td>
<td><strong>Tr</strong></td>
<td><strong>Clk x Tr</strong></td>
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<tr>
<td><strong>Clk</strong></td>
<td>1.20E+07</td>
<td>2.60E+09</td>
<td>3.00E+11</td>
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<tr>
<td><strong>Tr</strong></td>
<td>275,000</td>
<td>2,000,000,000</td>
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<td><strong>Clk x Tr</strong></td>
<td>3.30E+12</td>
<td>5.20E+18</td>
<td>8.25E+16</td>
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<tr>
<td><strong>Clk x Tr (Relative)</strong></td>
<td>6.35E-07</td>
<td>1.00E+00</td>
<td>1.59E-02</td>
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<tr>
<td><strong>Flops</strong></td>
<td>1.2E+05</td>
<td>4.0E+10</td>
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<td><strong>(M)IPS, Measured and Estimated</strong></td>
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<td><strong>Power Consumption</strong></td>
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<td>80</td>
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<td><strong>Energy / Instruction (J)</strong></td>
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<td><strong>Energy / Clock (J)</strong></td>
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<tr>
<td><strong>Energy / Clock (fJ)</strong></td>
<td>2.50E+08</td>
<td>3.08E+07</td>
<td>6.67E+07</td>
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<tr>
<td><strong>Energy / Clock (Relative)</strong></td>
<td>1</td>
<td>1</td>
<td>2.17E+00</td>
</tr>
</tbody>
</table>

250 x 250μm² o-Tr’s on 6” GaAs wafer

20 kW

Ultrafast Optical Logic Lab., UEC
optical-processor 80386 (with 300,000 gates)

advantage of serial-processor

latency, synchro issues → 1/100 or less
programming costs, risks → 1/100 or less

→→ technical efficiency → 100x / 15 yrs

serial-processor

1.0E+12
1.0E+13

parallel

1.0E+11
1.0E+10

optical-80386 (estim.)

• Clk: 100x
• MIPS: increases
• energy per clock: comparable (70 nJ/clk)

(all relative to Core2-quad)

Possible to integrate??
250 × 250μm² o-Tr’s
on 6” GaAs wafer
屛 275,000 Tr’s (=80386)

Previously,
Tr number × Clk: 100x / 8 yrs
FLOPS 100x / 8 yrs
MIPS 100x / 15 yrs

Ultrafast Optical Logic Lab., UEC
Summary (ssdm 2010)

- Impacts of ICT-related energy consumptions
e.g.: energy supply to Data centers in USA: 10 nuclear reactors
  heat energy from one server rack: 20-kW level.
  many-folded parallel-data-processes will the best for all applications, thru. 2050?

- <speed, energy, size> of all-optical gates, at present: <200G, 3 pJ/bit, length, 1 mm>

- <speed, energy, size>, 2nd or 3rd generation: <300G, 0.3 pJ, 250 µm²>

- in Materials Research (semi-classical quantum):
  optical acceleration (incl. gate scheme),
  electron-photon interaction (little studied),
  higher-density excitations (w/ larger hetero-barrier).

- optical-4004: MIPS, comparable to Core2 quad. Electric energy, 200W.
- optical-80386: 300,000 gates. Energy per clk, comparable to Core2 quad.
  (this will probably save energy and costs, for a group of serial-process-oriented tasks.)

  an alternative to 40-year-long Moore’s law
Thanks to Co-authors and Collaborations

Co-authors:
- Jun Sakaguchi, PhD course, UEC
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- Naoya Wada and Satoshi Shinada, NICT Labs.
- and several more.

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