

If anybody likes to keep this talk's slides, please email me!

Roadmap of ultrafast energy-saving *optical* semiconductor devices to Year 2025

--- <speed, energy, size> estimates of optical Micro Processor Unit ---

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Tokyo, Japan

42nd ssdm, Tokyo, Sept. 22, 2010

Contents

- [1] Total energy consumptions in ICT technology
- [2] Recent trends of optical-data-processing devices <speed, energy, size>
- [3] All-Optical gates: from principles to new potentials <speed, energy, size>
- [4] Crude estimates about “optical MPU” (long-term research)
(first time, too, to our knowledge)

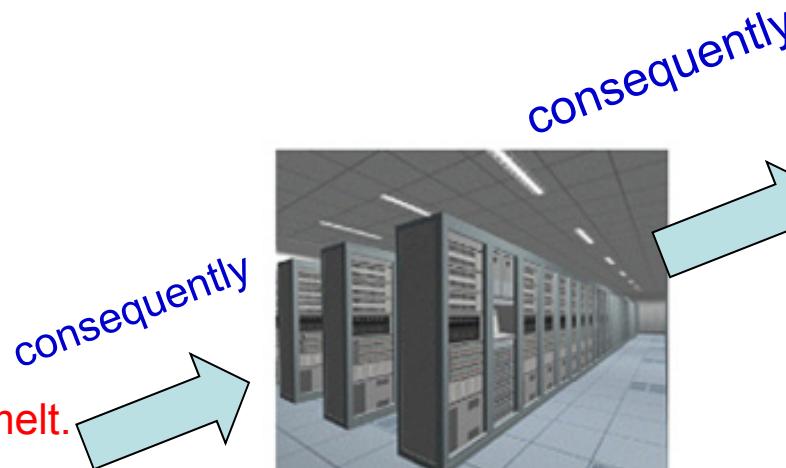
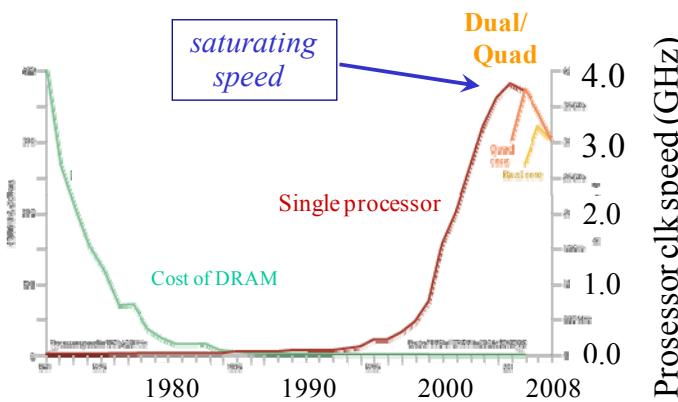
Co-authors and Collaborations

[1] Energy consumptions in ICT-related systems

Conventional Technol.
(electronic MPU's)

Around 2005,
Clk freq. reached 3 GHz.

Nano-materials inside MPU's are nearly melt.
(37 years of Moore's law, IEEE 2008)



Nuclear Power-Station
1 GW / reactor

In **Data Centers** of Google, Microsoft, etc.

Clk freq.: 3 GHz, with similar MPU's

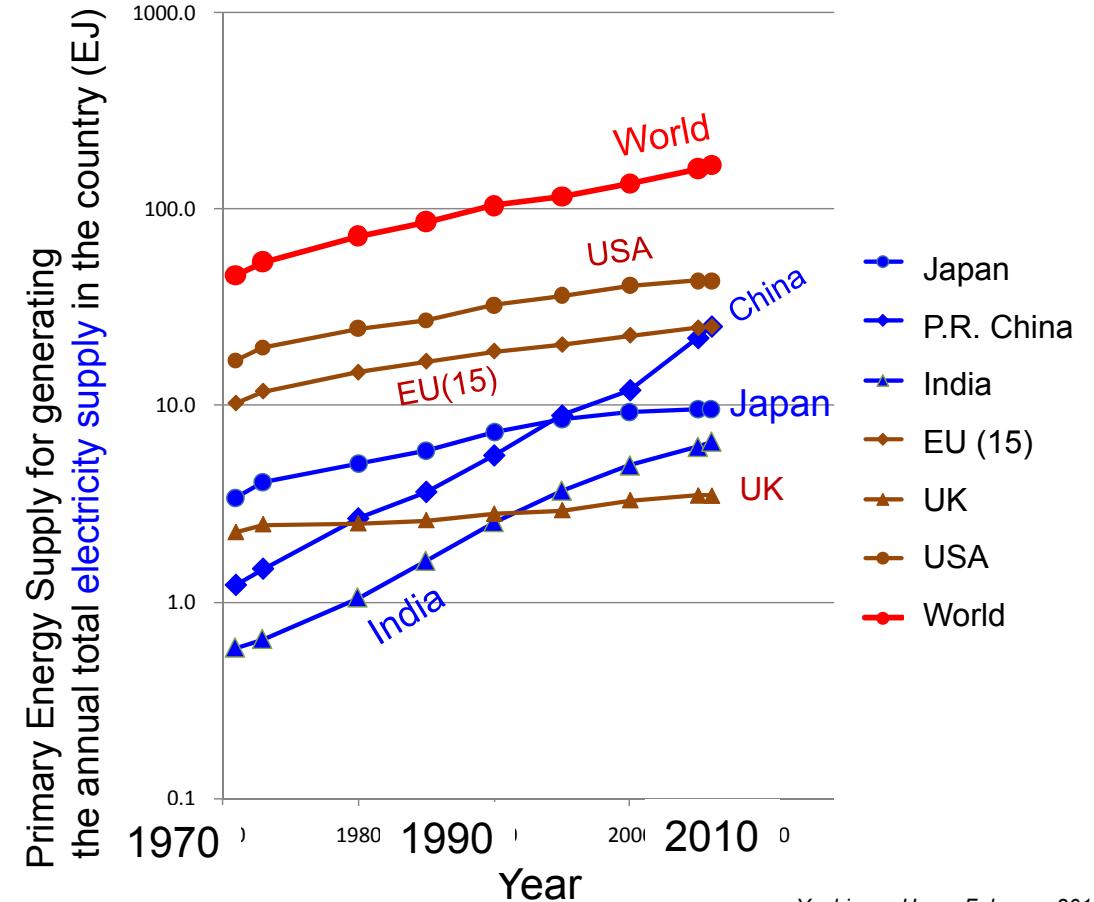
Heat-energy dissipation: 10 kW / sever rack

Data-center energy: 20 MW / data center

We need ultrafast & energy-saving
Optical Transistors
in future !

Electric-energy consumptions, 1970-2006

Primary energy supply, for electricity



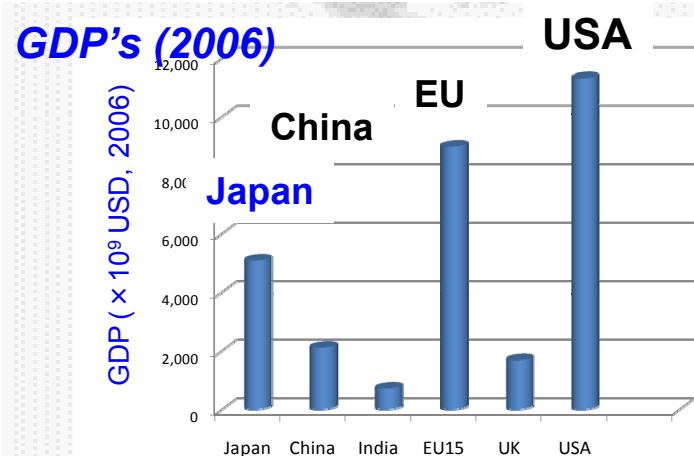
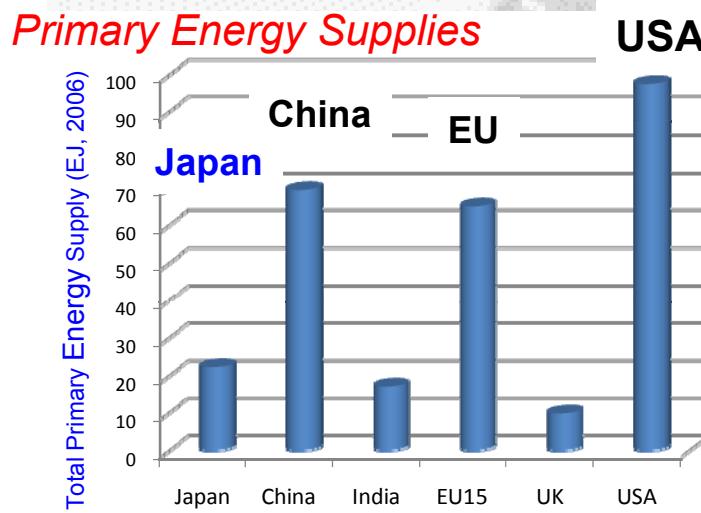
*1) Source: International Energy Agency (IEA), Paris,
Energy balances of OECD countries and non-OECD countries.

*2) 1 EJ = 1×10^{18} J.

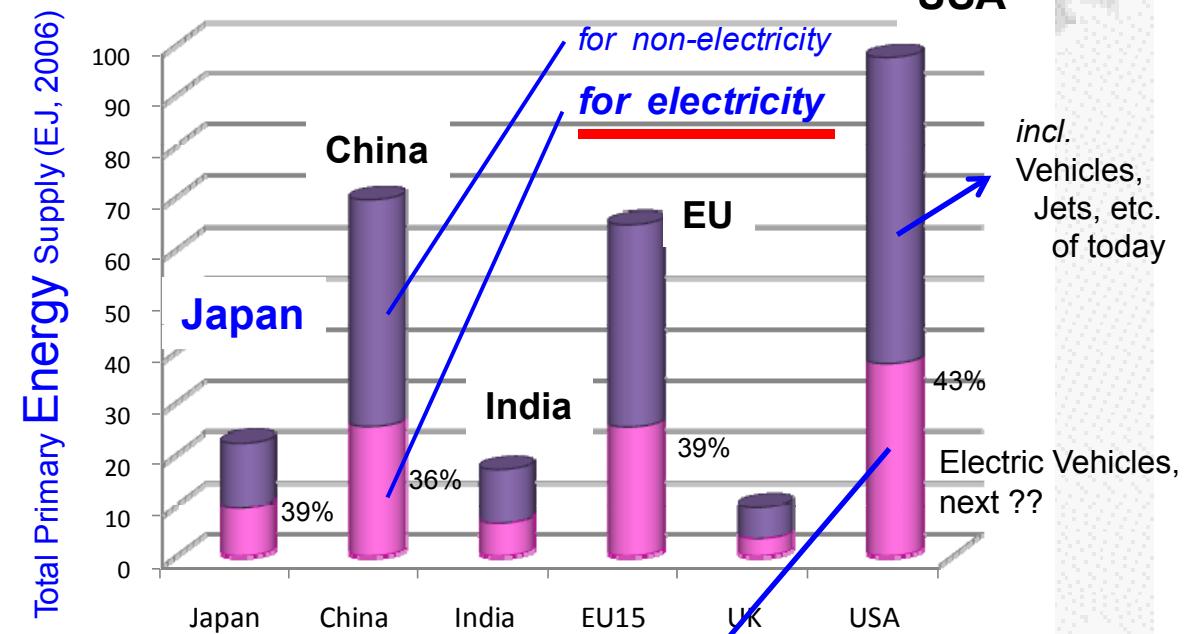
[1] Impacts of ICT energy consumptions

Macro-scoptic:

Primary Energy Supplies (sum of electricity and non-electricity), 2006



Ratios of energy for electricity

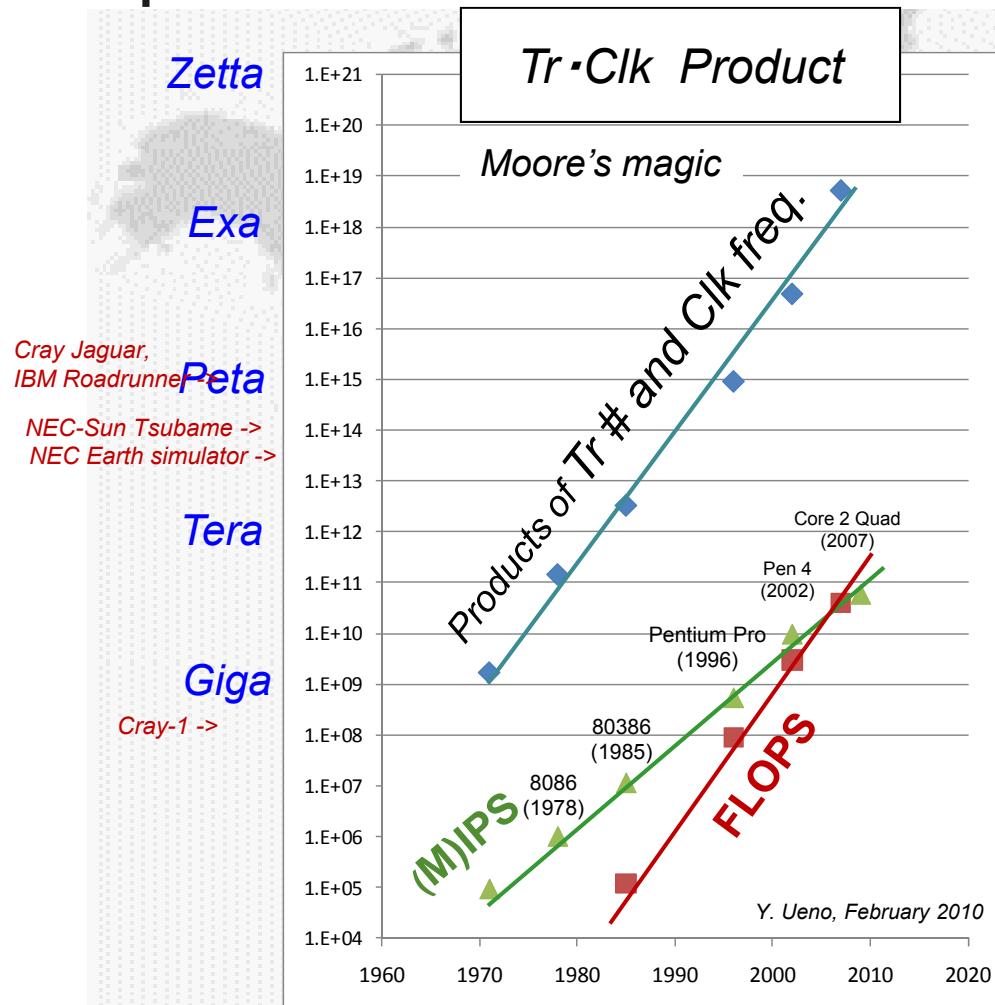


*1) Source: International Energy Agency (IEA), Paris,
Energy balances of OECD countries and non-OECD countries.
*2) 1 EJ = 1×10^{18} J.

Data Centers in USA consuming 1.5% of all electricity (D. Miller, Stanford).
not very large?? → 1.5% corresponds to **10 nuclear reactors!!**
→ We need energy-saving devices.

Micro-scopic:

one origin of ICT-energy consumptions



Tr-number times Clk-freq. has evolved
by a factor of $10^6 \times 10^4 = \underline{\underline{10^{10}}}$ (in 40 years)

Tr number: 10^6
Clk freq.: 10^4

- FLOPS speed has increased by 10^{10} .
- MIPS speed has increased by 10^4 , only, without supported by Tr number. (reasonable)
- Already relying on parallel-processing MPU's and software. many-folded parallel-structures are probably pushing-up electric-energy consumptions (and costs). [hard to quantitatively characterize now, though.]

? for 2010-2050: Increasing demands are
FLOPS-type demands, or, MIPS-type demands ??

- ◆ no. of Trs. times clk freq. 10x every 4 yrs.
- FLOPS 10x every 4 yrs.
- ▲ Instructions per sec. 10x every 7 yrs.

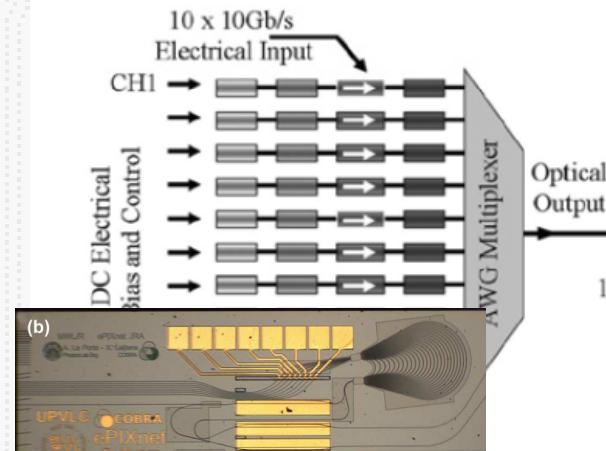
to move from electronics to optics: its famous weakness

Latest degrees of integrations for optical-processing devices

Number of devices on one chip = **200** (Infinera, 2006)

→ evolving steadily, driven by industrial demands,

and approaching the number 2,300 in intel 4004 (1971).



Eindhoven Univ. Technol., Netherlands

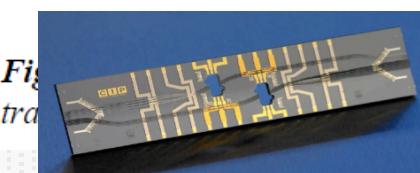
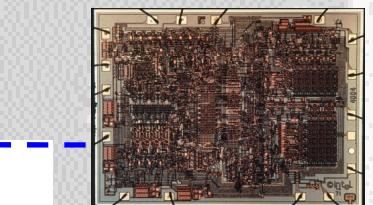
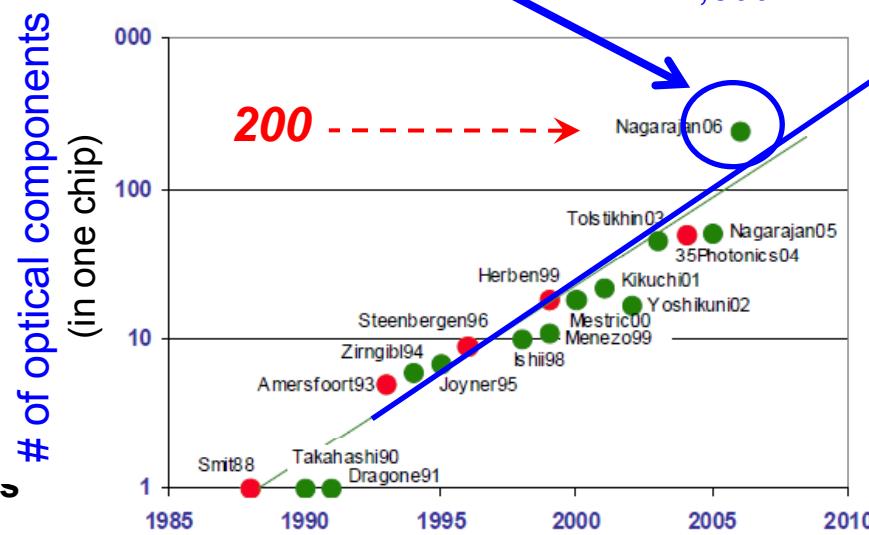


Fig. 1 IC: a WDM transponder in Infinera [1]

CIP Technologies, UK.



Electronic processor
Intel 4004 (1971)

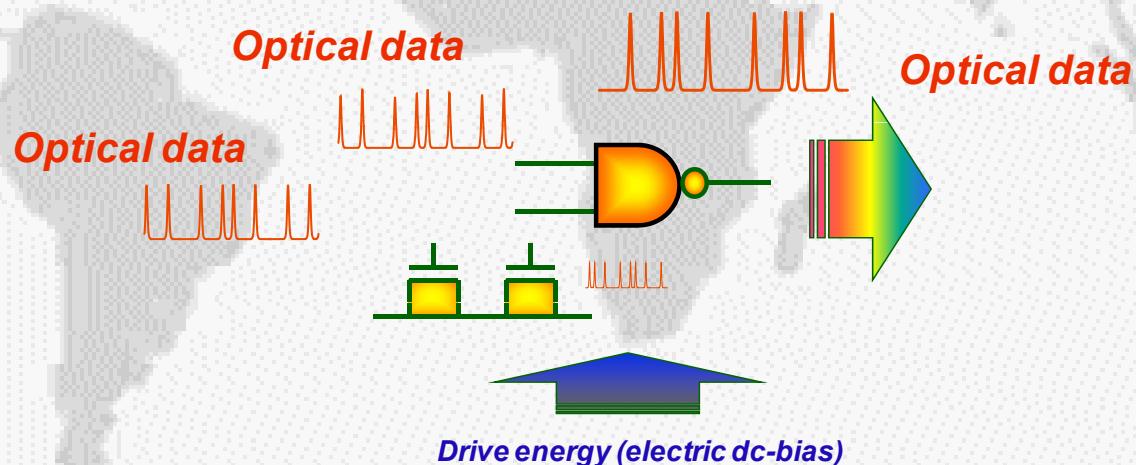
source:

M.K. Smit (Eindhoven U. Technol.), IEEE-LEOS Annual 2008.

[2] Optical-data-processing “gates and memories”

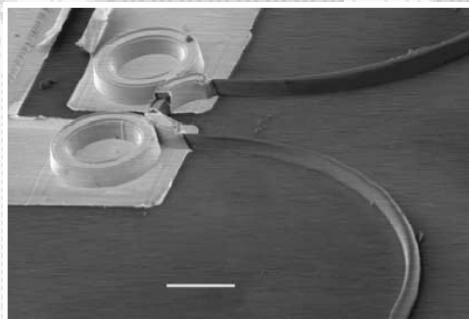
All-Optical circuits w/ gates & memories

Y. Ueno, UEC, 2010

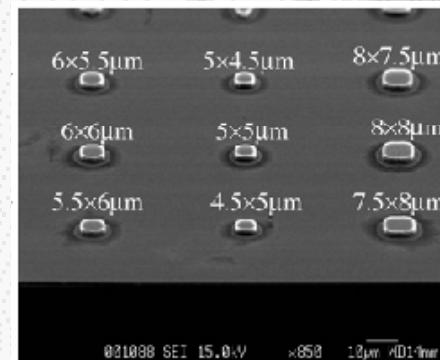


[2] Optical-data-processing “gates and memories” <speed, energy, size>

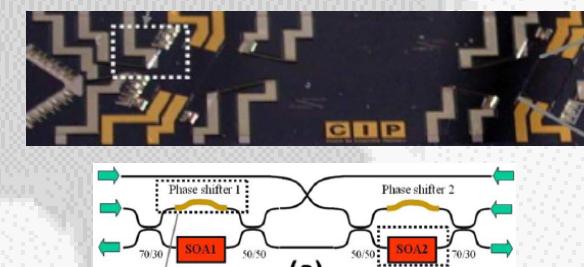
(2-1) Optical buffer memories (fundamental-research)



25Gb/s, 1pJ/bit, $(30\mu\text{m})^2$
M.T. Hill (Smit Gr., Eindhoven),
planar, ring-laser.

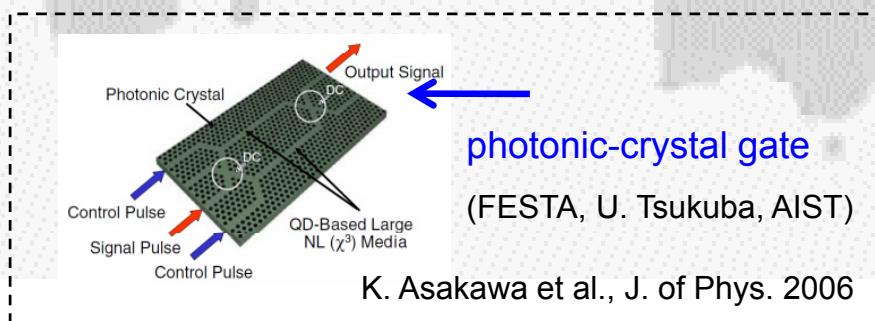


40-100Gb/s, 3pJ/bit, $(10\mu\text{m})^2$
T. Katayama (Kawaguchi Gr.), 2009,
Vertical, VCSEL.



40-160Gb/s, L= few mm long
E. Kehayas (Dorren Gr., Eindhoven)
planar, coupled-gates.

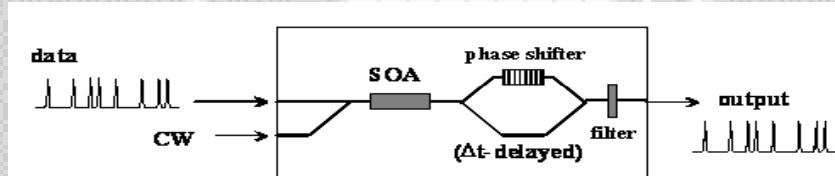
photon-electron interactions
In bulk or MQW semiconductors
are used.



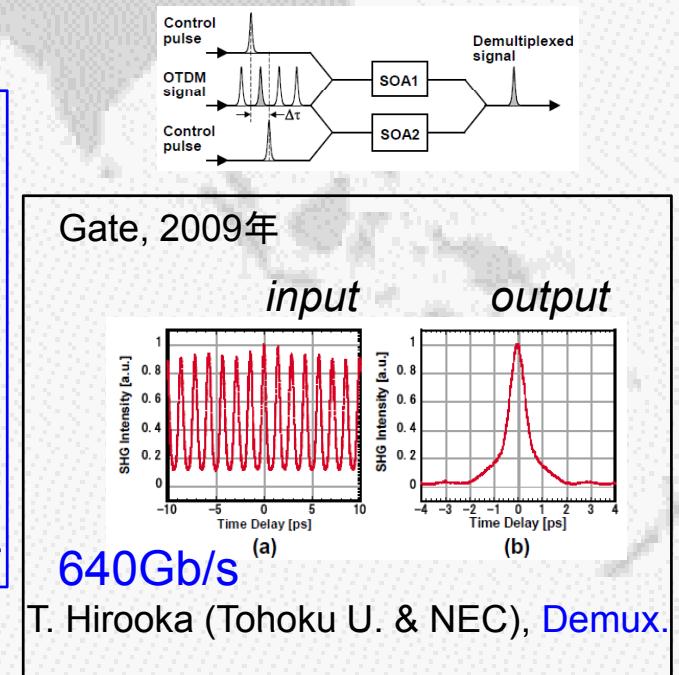
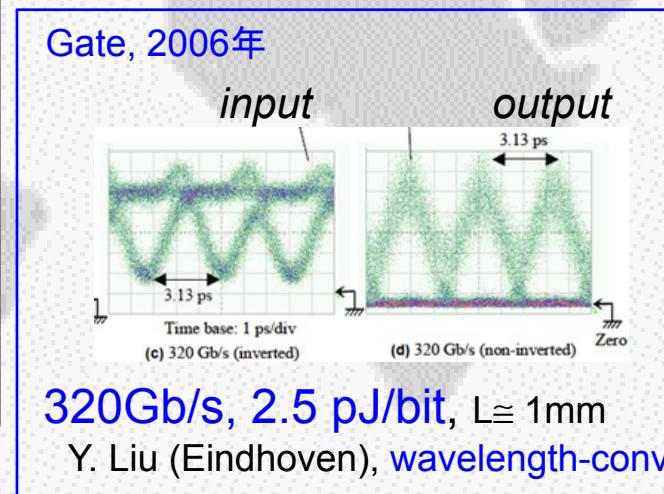
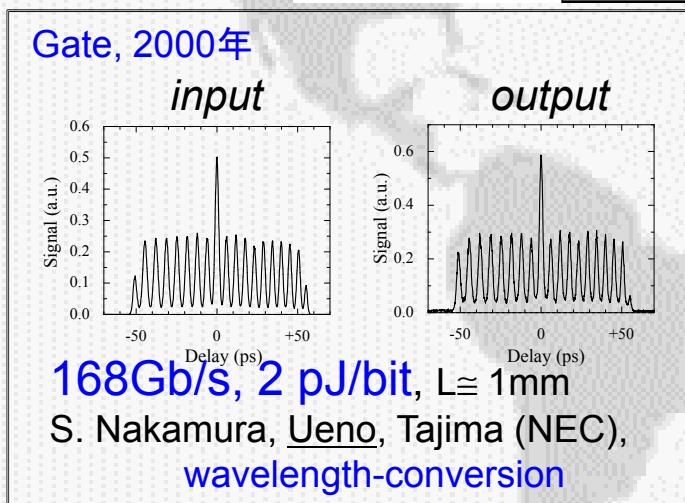
[2] Optical-data-processing “gates and memories” <speed, energy, size>

(2-2) All-optical gates (for practical signal-conversion, 2R/3R, demux, etc.)

SMZ-DISC scheme, with non-linear cross-phase modulation XPM



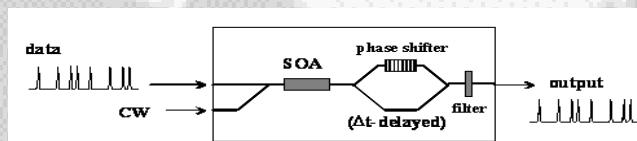
original-SMZ scheme, with XPM



[2] Optical-data-processing “gates and memories” <speed, energy, size>

(2-2) All-optical gate (fundamental-research in our univ. UEC, Tokyo)

SMZ-DISC scheme (XPM) in our group

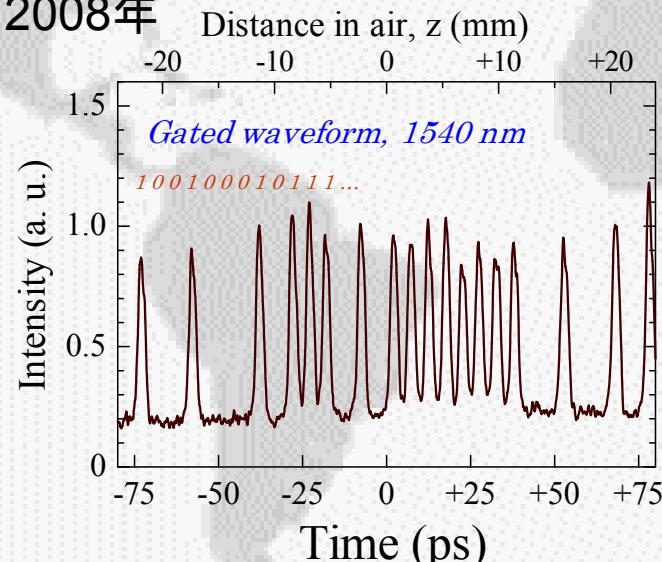


→ Converter, XOR, AND, 2R/3R, etc.

→ Flip-Flop (Eindhoven, Tsukuba)

→ Clock oscillator (UEC)

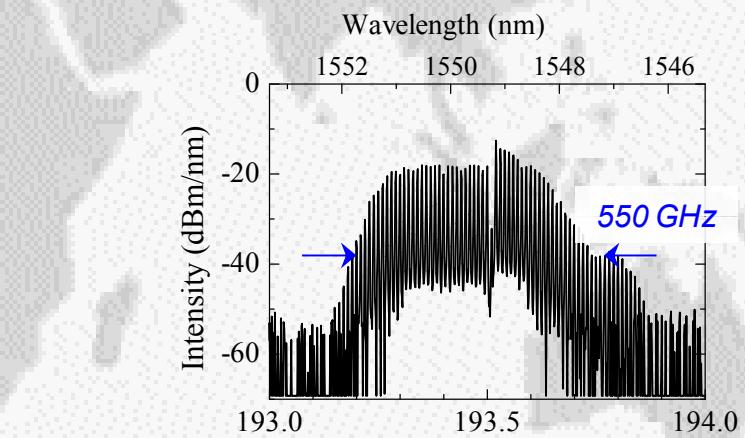
Gate, 2008年



200Gb/s, 3 pJ/bit, L ≤ 1mm

Sakaguchi, et al. (Opt. Comm. 2009)

Oscillator, 2005-2008年

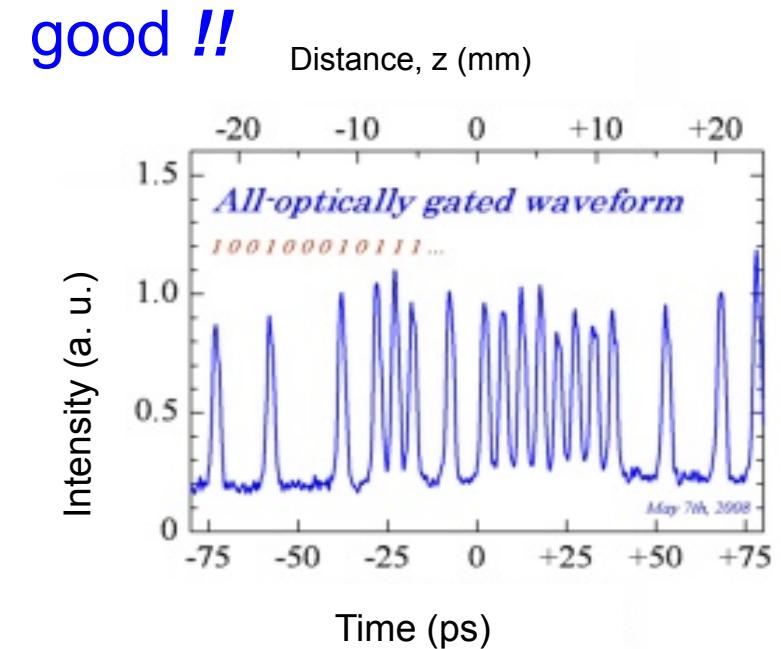
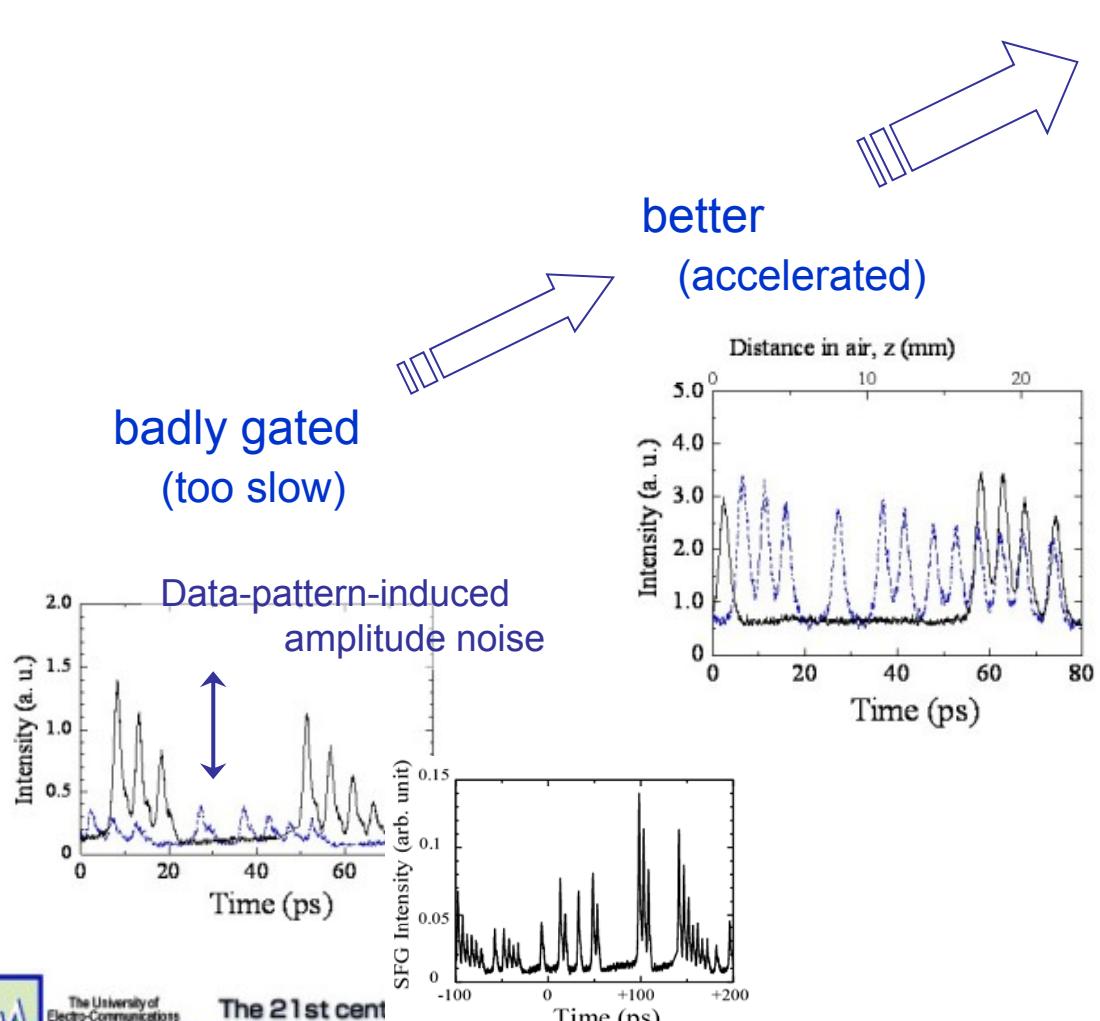


Δ2ps/40GHz optical clock oscillator

Suzuki, Nakamoto, et al. (CLEO2006, NANO2d08)

200-Gb/s gated waveforms,
in the middle of our experimental studies

Jun Sakaguchi, et al., Opt. Comm. 2009.

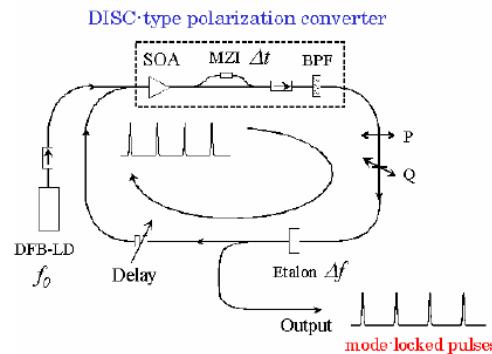


Clock oscillator (UEC)

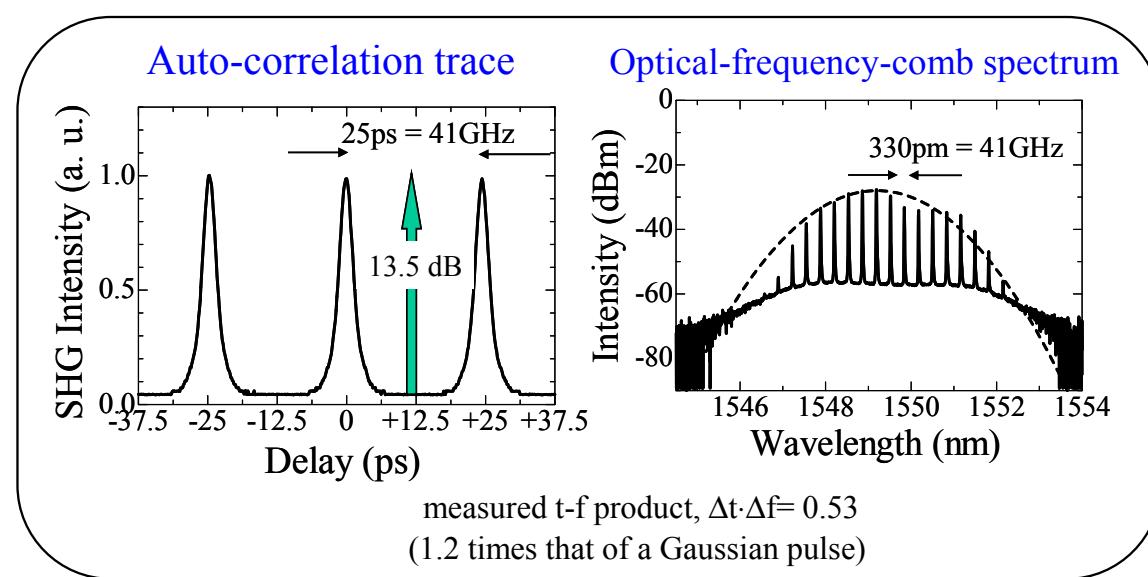
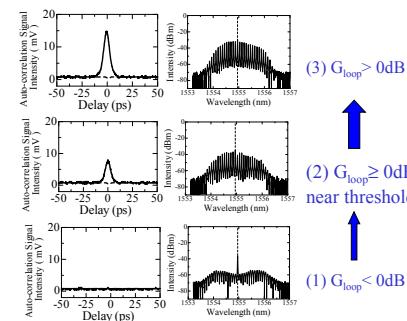
COE-research: DISC-loop-type mode-locked pulse source

2-ps, 40-GHz pulse and comb generation, 2005-2006

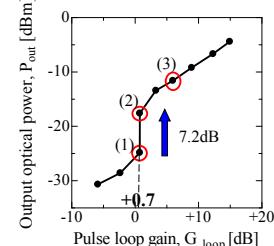
R. Suzuki, et al., CLEO, Long Beach, USA, May 2006.



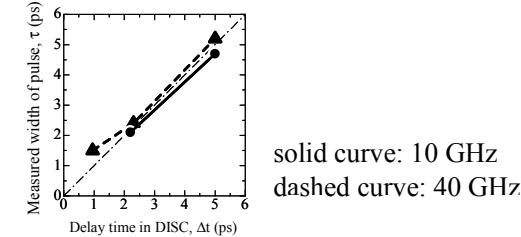
Original scheme from,
Y. Ueno, et al., Appl. Phys. Lett. Oct. 2001



Proof of principle (1), threshold behavior



Proof of principle (2), linearly controlled pulse widths



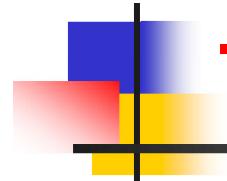
The 21st century COE Program
Innovation in Coherent Optical Science

Ultrafast Optical Logic Lab., UEC

fundamental research of “gates”

→ XOR, AND, 2R/3R, etc.
 → Flip-Flop (Eindhoven, Tsukuba)
 → Clock oscillator

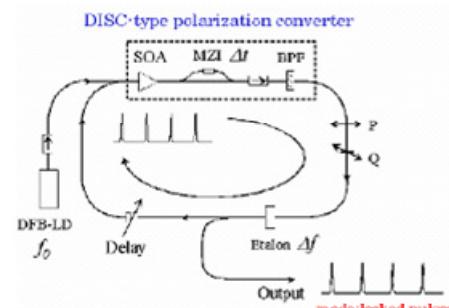
Clock oscillator (UEC)



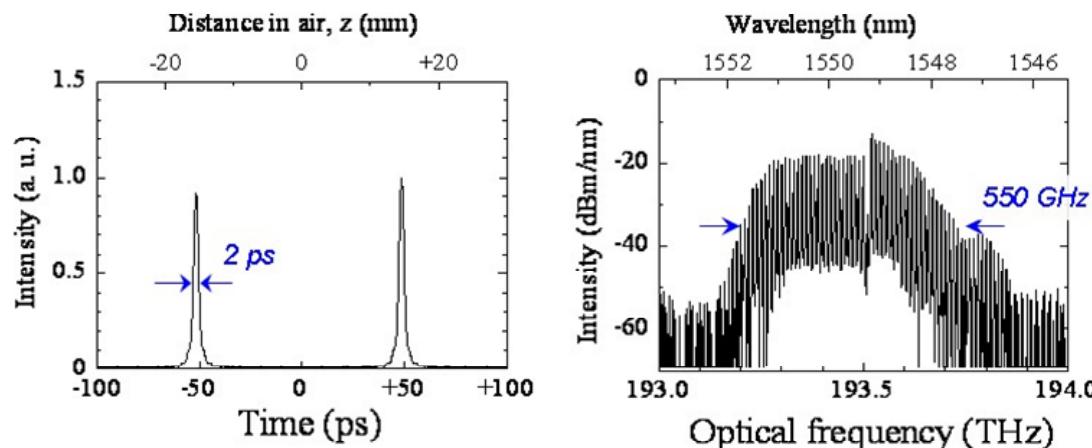
single-longitudinal-mode mode-locking, 2008

(with using high-Q etalon filter designed by JAE Japan)

precise, only-one-mode lasing
 out of $\Delta 10\text{-MHz}$ -spacing modes.
 (Nakamoto, et al. OSA-NANO 2008)



Original scheme from,
 Y. Ueno, et al., Appl. Phys. Lett. Oct. 2001

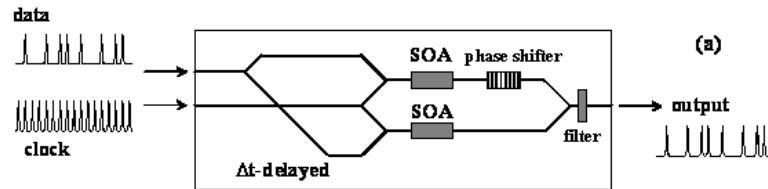


Original features of this scheme of ours:

- 500-GHz-BW comb, low power consumption, integration possibility (*presently*)
- precise optical frequency, f_{opt} (locked to external DFB source, f_{opt})
- precise repetition frequency, f_R (locked to dielectric etalon's FSR, f_R)
- precise comb envelope shape, f_{BW} (locked to dielectric MZI delay time, Δt)

fairly-good

status of Modeling-research (optical gates)

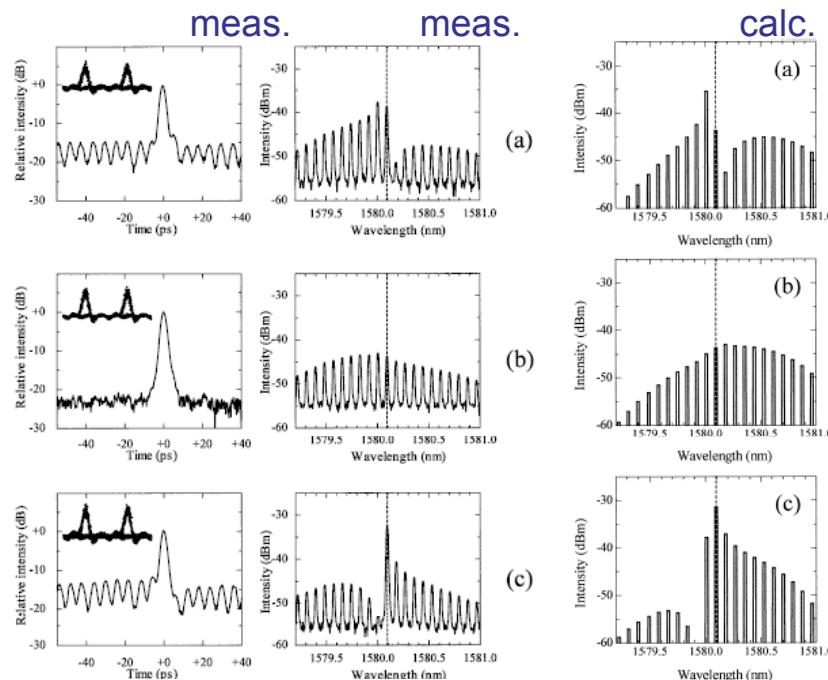


Ueno et al., 2001-2002
ECOC, IE³ PTL, IEICE Trans.

from the hybrid-integrated SMZ device

Subject: about the useful correlation between
sensitive dependences of waveform and spectrum, on the optical phase bias, $\Delta\Phi_B$

waveforms
in the log scale

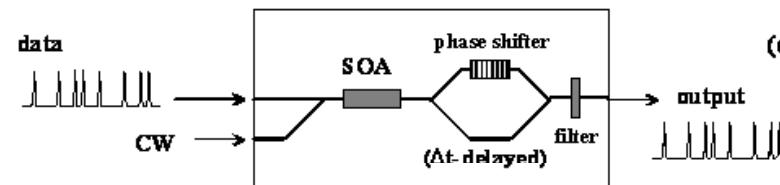


Conclusion:
we'll be able to feedback-control
the 160-Gb/s Demux
by monitoring the “supervisory” spectrum

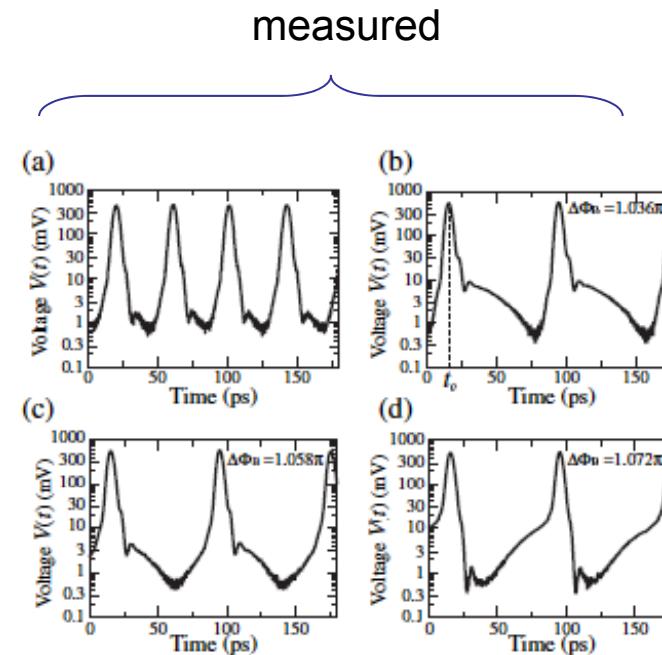
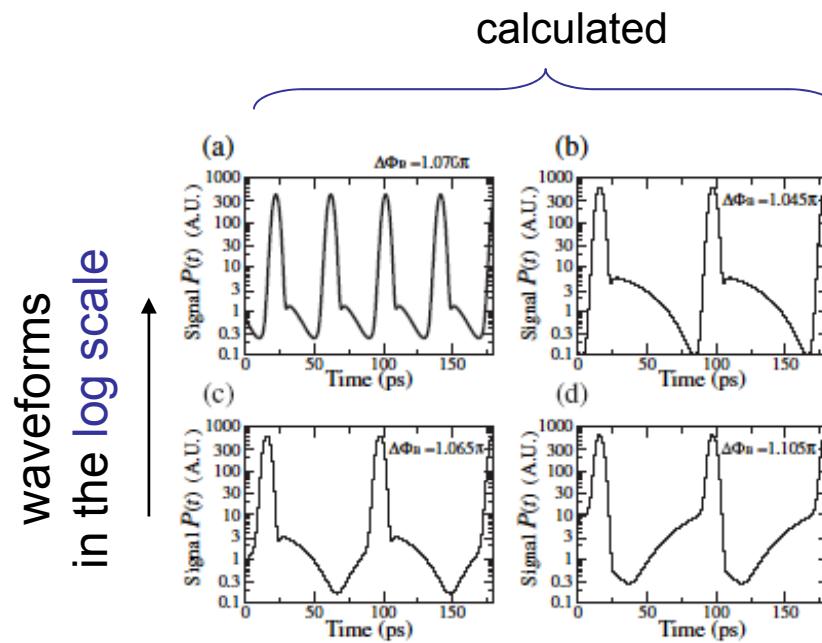
fairly-good

status of Modeling-research (optical gates)

J. Sakaguchi et al., JJAP 2005 and 2008



(c) subject: about one generic issue for DATA conv.
in the original DISC design

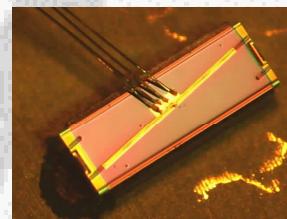


To solve this, within DISC scheme, we need a kind of imbalance factor between the two interferometer arms.

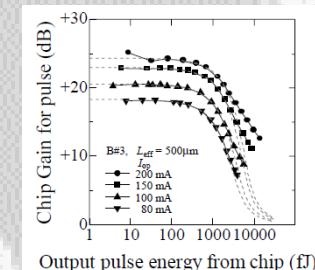
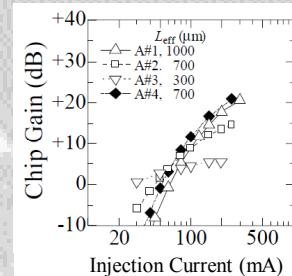
[3] Physics and potentials, of all-optical gates <speed, energy, size>

Quote: "All-optical semiconductor gate seems *too complicated*"

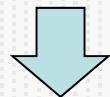
--- Prof. Guifang LI, CREOL/UCF, USA.



Inversion-population semiconductors (SOA's)

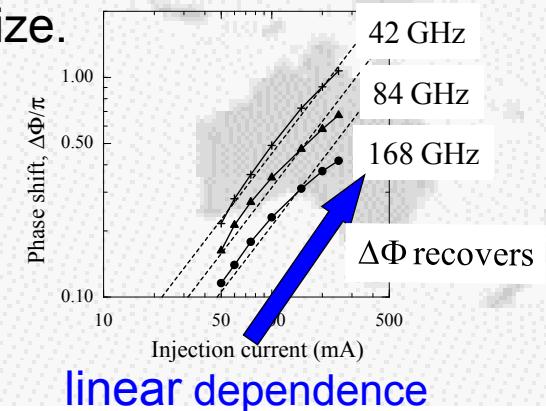


- nonlinear dependences → unsaturated gain G_0 , gain-saturation energy P_{sat} , optical 3R/2R.
- linear dependences (many ways) → in gate speed, energy, size.



Ueno et al., JOSAB 2002

"not so complicated !!"

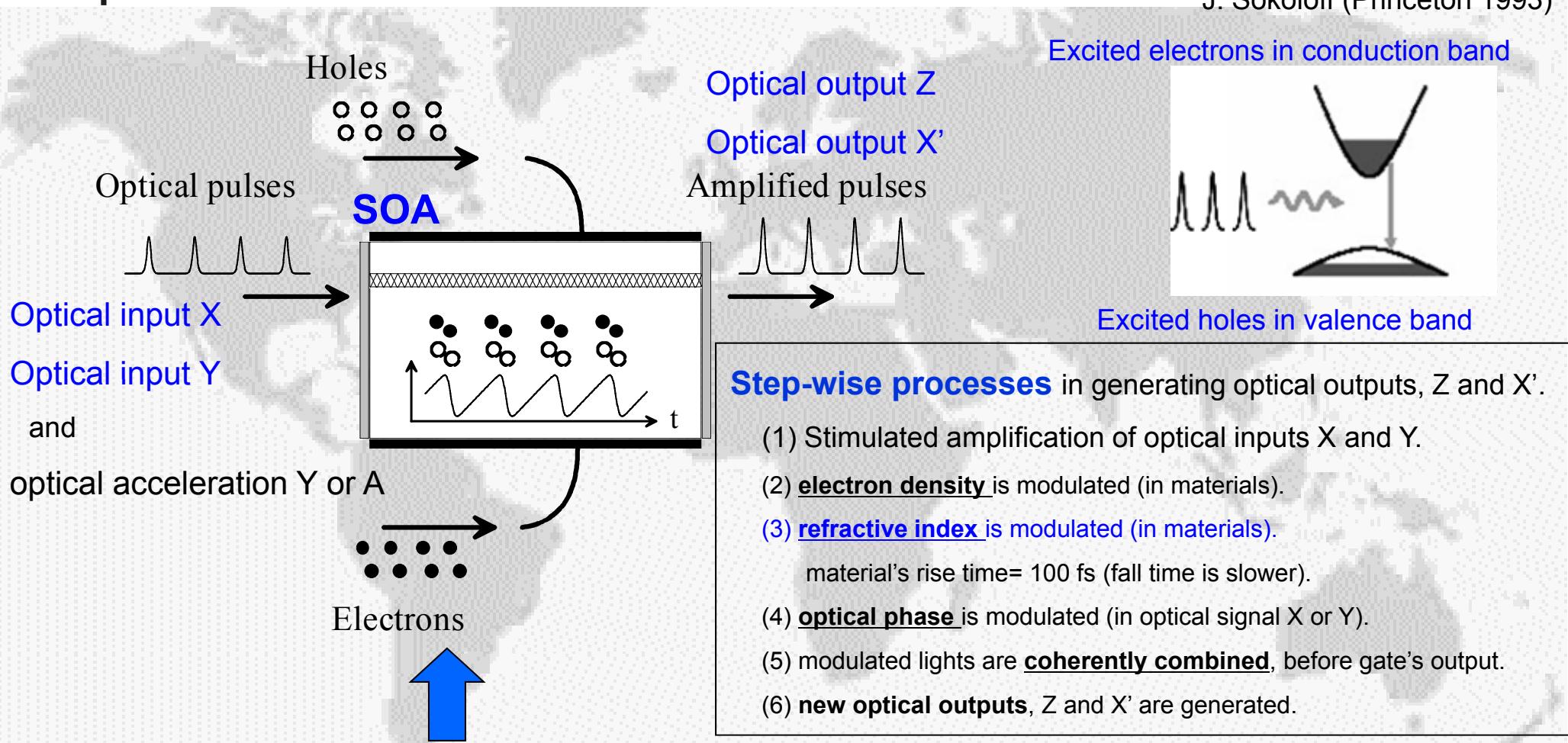


Physics : Refractive-index modulations, etc.,

due to excited-electron-hole-density modulations

K. Tajima (NEC 1993)

J. Sokoloff (Princeton 1993)



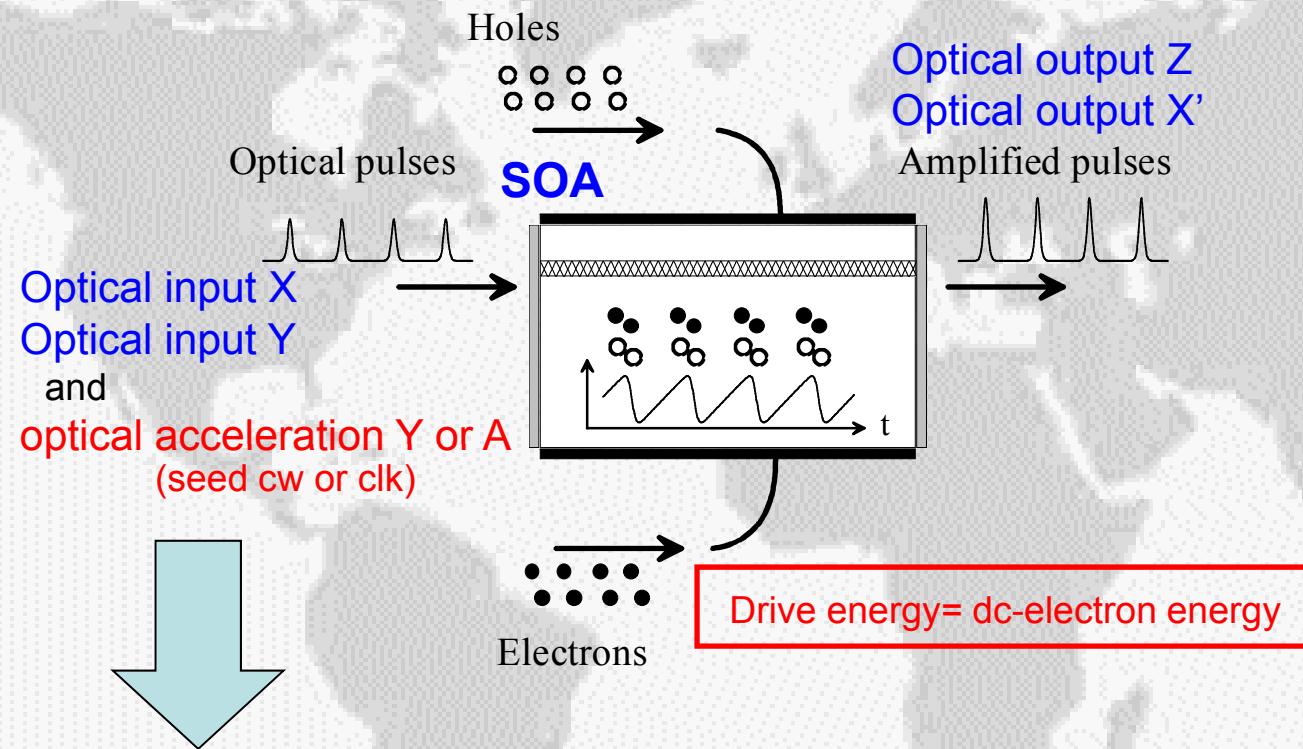
Drive energy= dc-electron-injection energy (dc-bias current)

[3] All-optical gates/ speed

Speed of gates

faster than material-relax. speed,
after optically accelerating the material

Origin: R. Manning (BT), EL 1994



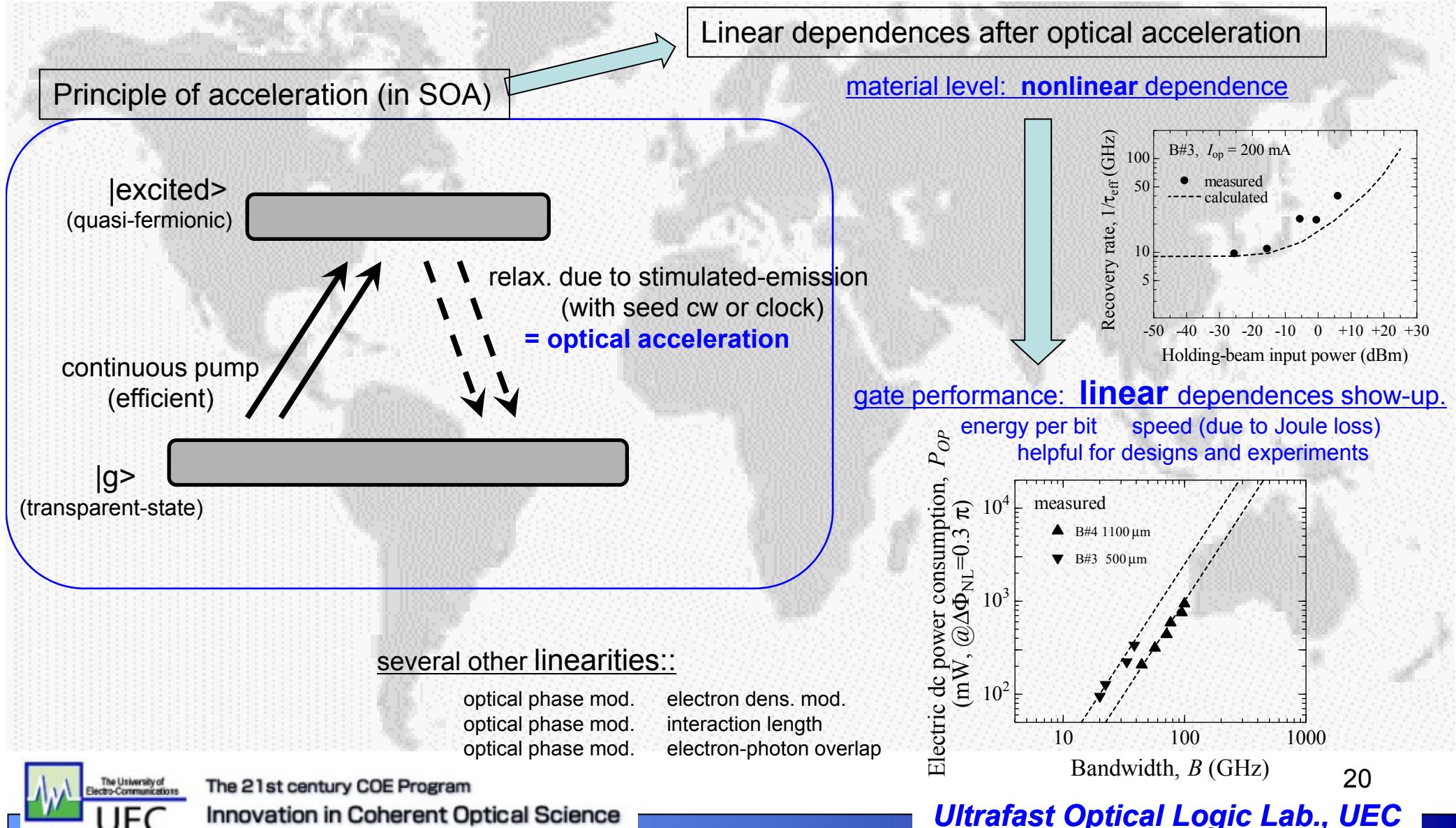
- For gates, this acceleration is equivalent to “faster materials”
- Energy consumption is equivalent to them, as well.

} *experimentally recognized.*
(Sakaguchi, et al., Opt. Express 2007)

$$\frac{d}{dt} n_c = \frac{I_{op}}{qV} - \frac{\{G[n_c] - 1\}}{V} \times \frac{|E_{accel}(t)| + |E_{data}(t)|^2}{\hbar\omega}$$

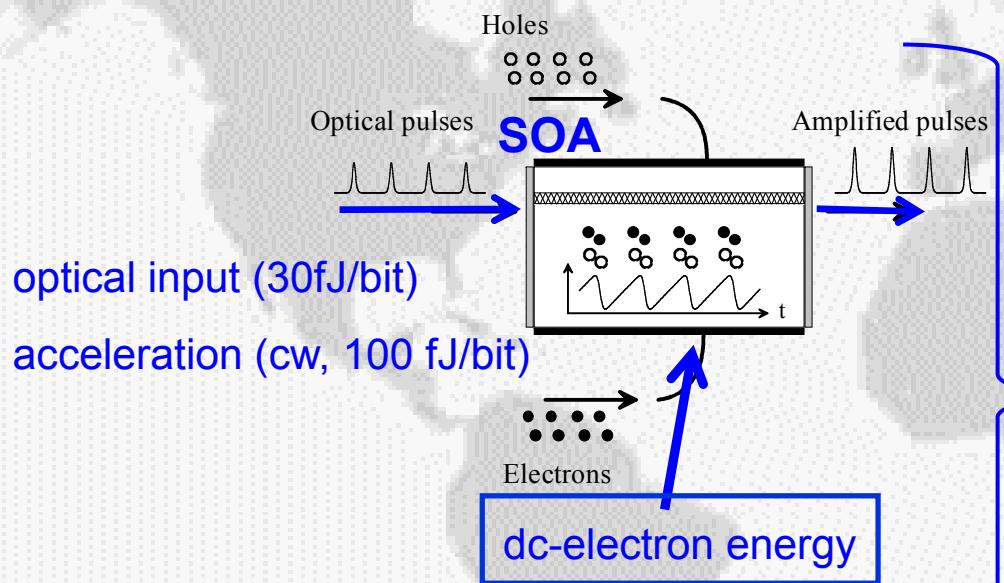
Speed of gates, more simply

Sakaguchi, et al., Opt. Express 2007
Ueno et al., JOSAB 2002



Speed of gates → numbers at operating point (200Gb/s)

Principle of gate = electron-pump



- electron consumption = 1×10^7 electrons/bit
- electric-energy consumption = 3 pJ/bit

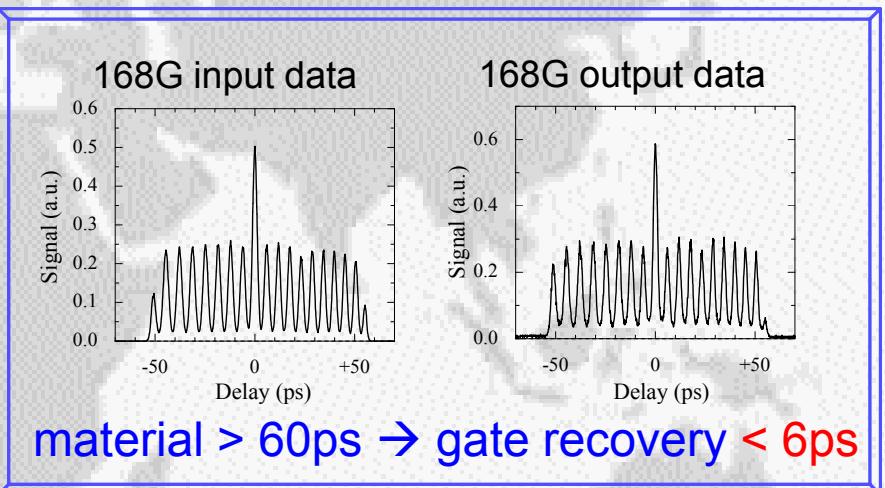
nearly-regardless of material's speed (in this regime)

w/ nonlinear pol. rot.

S. Nakamura et al., Appl. Phys. Lett. 2001

J. Sakaguchi et al., Opt. Comm. May 2009

168G wavelength conversion (2000)



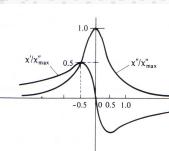
Energy-efficiency of gates → new potentials in near-future (--2025)

Other institutes: packet-routing, buffer memories, integrated 2R-subsystem.

300 pJ/bit
30 pJ/bit
(previously)

Our group (UEC): following directions (for energy-saving)

- blue-shift filter → Nielsen et al., Opt. Express 2006
- nonlinear-polarization rotation → Sakaguchi et al., Opt. Comm. 2009
- spectral-synthesis scheme → going-on (Nishida et al., IEEE-LEOS 2009)
(UEC-NICT collaboration, FY2007-)
- (non-deg. ->) degenerate-scheme → going-on
[free from polarization-insensitivity requirements]



3 pJ/bit
(present)

0.3 pJ/bit
(near future)

not yet started but, from near-future

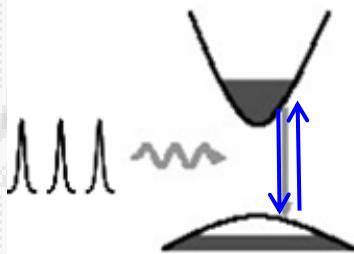
- QW-band-engineering, for enhancing refractive-index mod.
(e.g., ACQW)

further

- efficient pump (optical)
- low-dim., surface plasmon, nano-photo

100-fJ to 30-fJ
(far future)

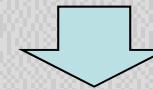
Size of gates → interaction L, new potentials in near-future (--2025)



dc-electron pump (at present)

energy supply of 3 pJ/bit , that is, $1 \times 10^7/\text{bit}$ of electrons, in interaction length= 1 mm

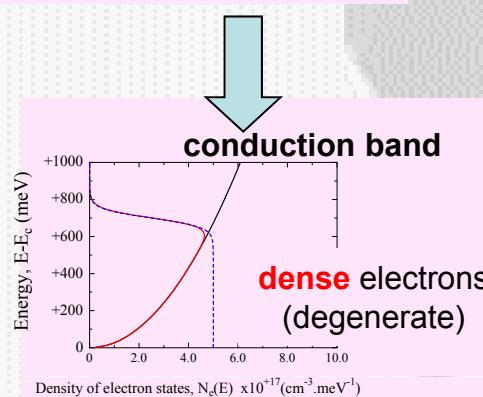
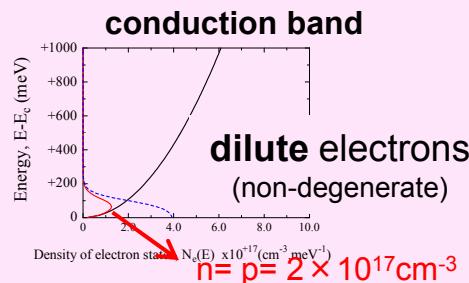
Volume density of excited electrons $> 2 \times 10^{18} \text{ cm}^{-3}$?



experimentally: stock= relatively dilute ($2 \times 10^{17} \text{ cm}^{-3}$) !

Sakaguchi et al., Optics Express 2007 through present

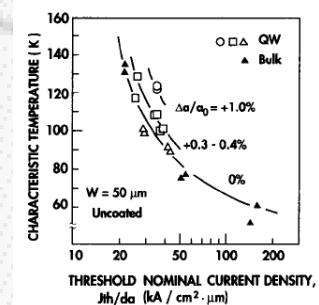
→→ flow (modulation)= less efficient (at present)



one of new potentials

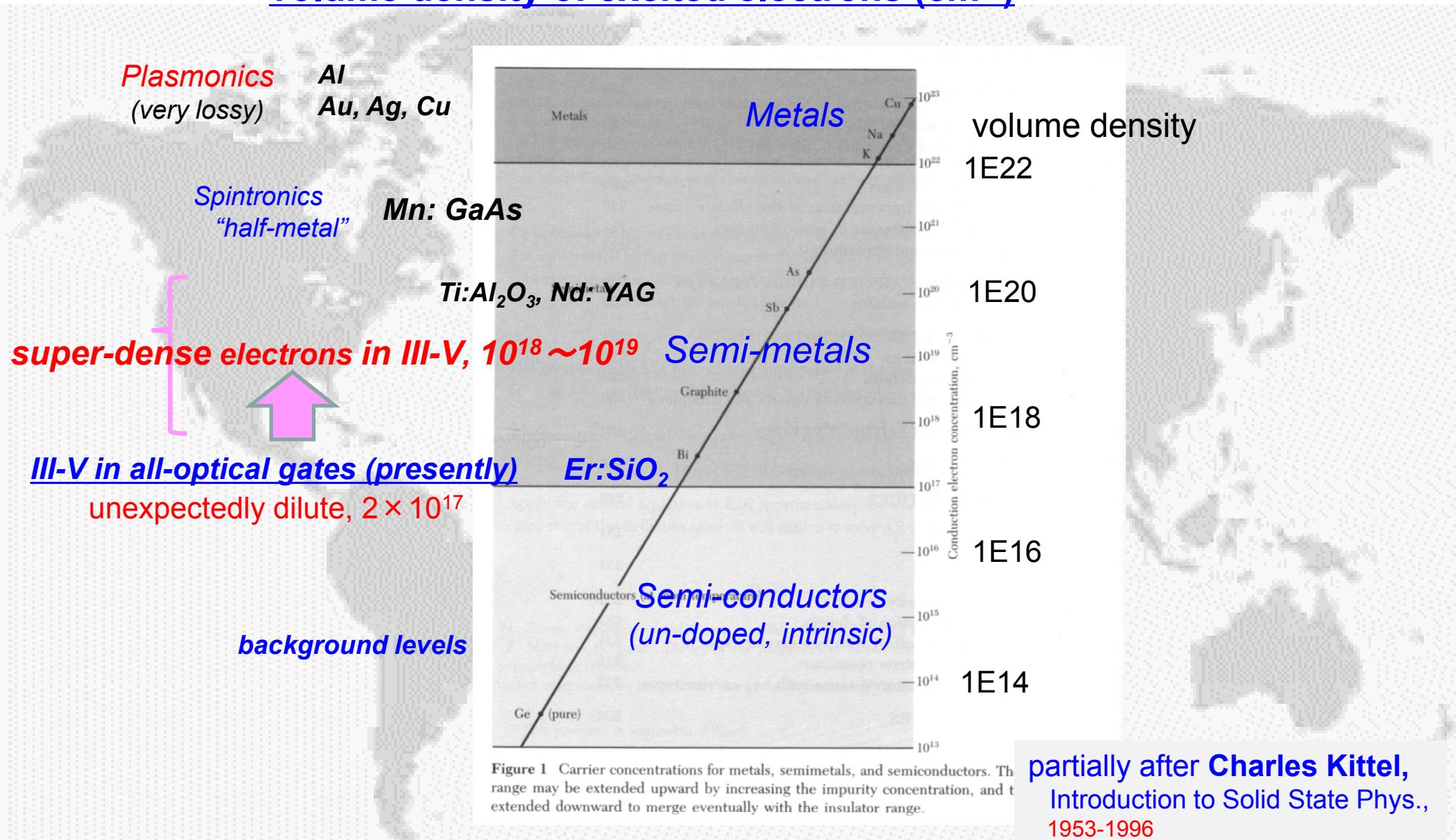
10-times more electron density ($2 \times 10^{18} \text{ cm}^{-3}$),
→ 10-times shorter gate length ($L = 100 \mu\text{m}$)

(Hetero-barrier energy seems not enough, at present)



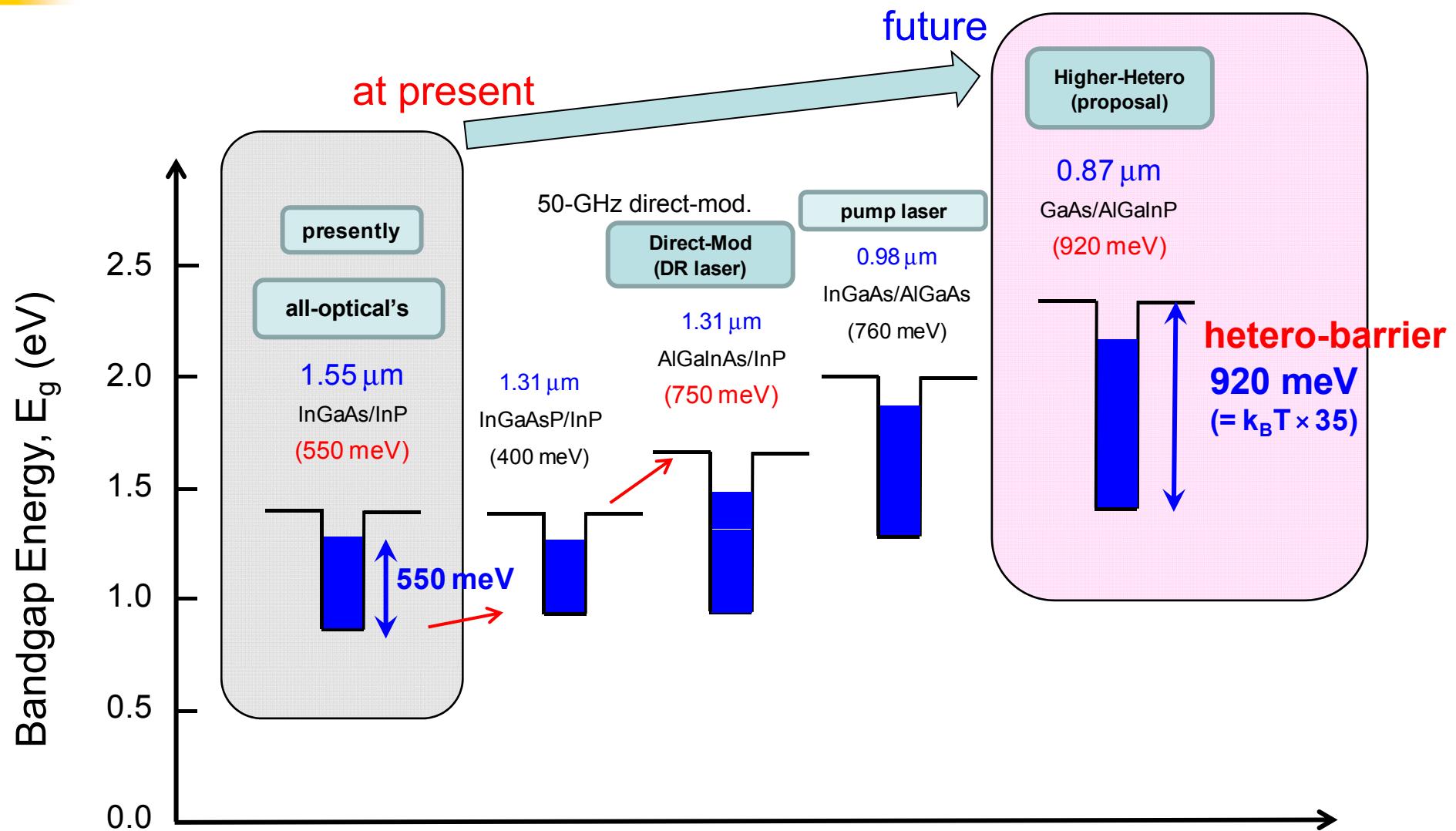
Characteristic temperatures
(AlGaNP/GaInP laser, 1993)

volume density of excited electrons (cm^{-3})



Super-high-density electron-confinement, with new hetero-barrier systems

[3] All-optical gates/ **size**



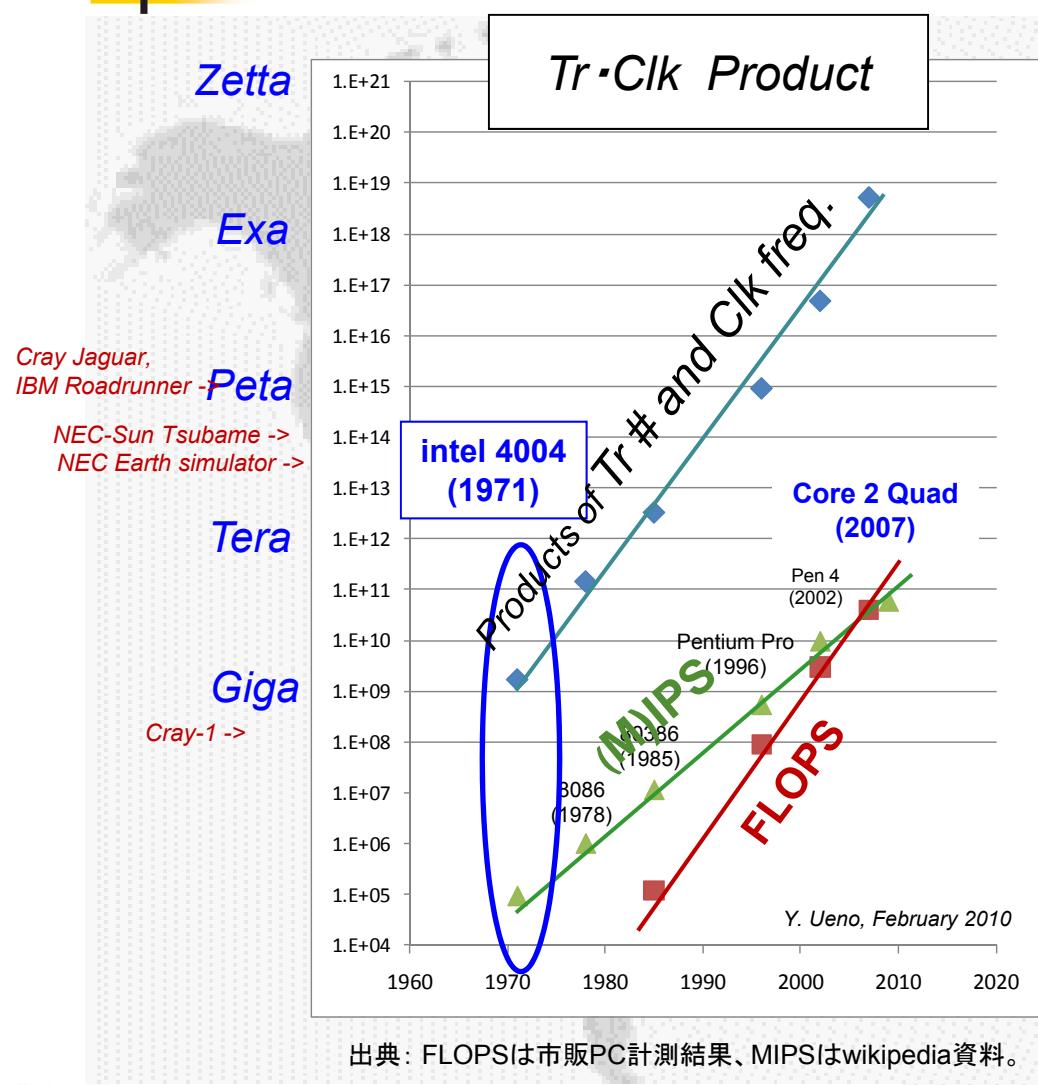
[4] Optical micro-processor, near Year 2025

near-future <speed=300G, energy=0.3pJ/bit, size(interaction)= 100μm>

Specification	Electronic	Optical processor	
	intel 4004	Present	Near Future
Demo Year	Year 1971	Year 2000-2010	Year 2025
Speed	500 kb/s	200-300 Gb/s	300 Gb/s
Energy (per bit)		3-10 pJ /bit/gate	0.3 pJ /bit/gate
Size (per gate)	70×70 μm ²	1,000×3,000 μm ²	500×500 μm ² (w/ 100-μm interaction)
Number of gates (per chip)	2,300 transistors	several	2,300 gates (6 chips on 3-inch wafer)
Energy dissipation (per chip)			200 Watt

Optical processor 4004

Relative performance of optical-processor 4004



Earlier statements:

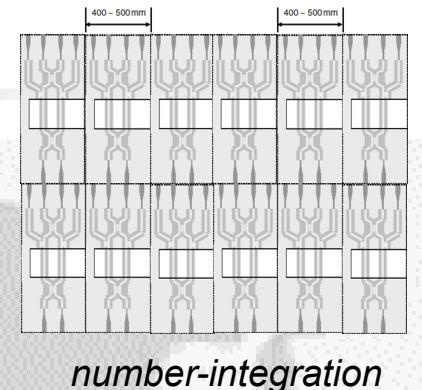
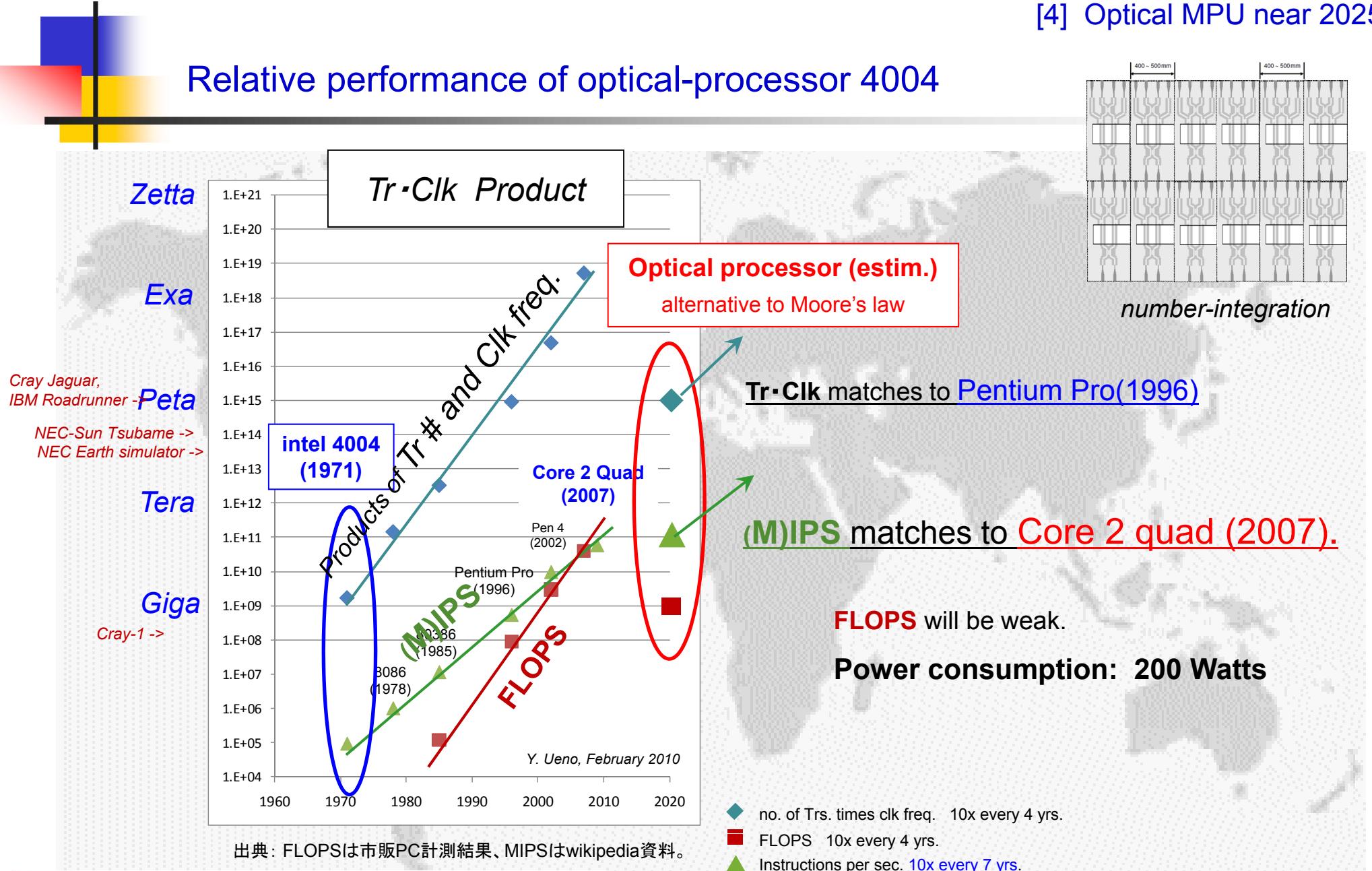
- already relying on parallel-processing structures, which are probably pushing-up their electric-energy consumptions.
- Increasing demands in 2010-2050 are FLOPS-type demands or MIPS-type demands??

◆ no. of Trs. times clk freq. 10x every 4 yrs.

■ FLOPS 10x every 4 yrs.

▲ Instructions per sec. 10x every 7 yrs.

Relative performance of optical-processor 4004



sample-spec. numbers of optical-80386



$250 \times 250\mu\text{m}^2$ o-Tr's
on 6" GaAs wafer

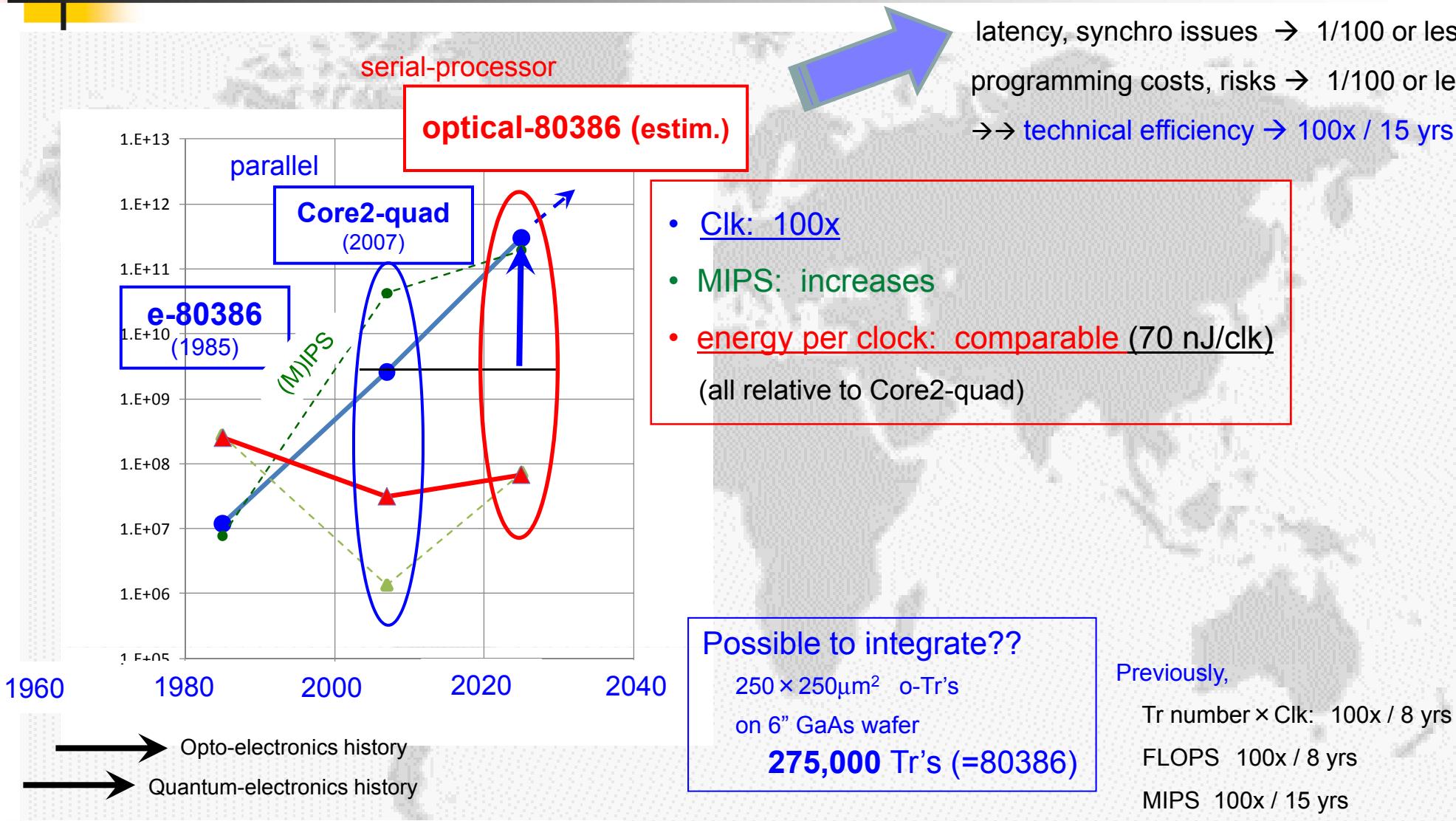
		e-80386 (32bit)	e-Core2_quad (32bit/64bit)	optical 80386 (32bit)	
	unit				
1	Clk	Hz	1.20E+07	2.60E+09	3.00E+11
2	Tr		275,000	2,000,000,000	275,000
	Clk*Tr		3.30E+12	5.20E+18	8.25E+16
	Clk*Tr (relative)		6.35E-07	1.00E+00	1.59E-02
3	Flops		1.2E+05	4.0E+10	-
4	(M)IPS, measured and estimated		1.10E+07	6.00E+10	2.75E+11
	(M)IPS (relative)		1.83E-04	1.00E+00	4.58E+00
5	power consumption	Watt	3	80	2.00E+04
6	energy / instruction	J	2.73E-07	1.33E-09	7.27E-08
	energy / instruction	fJ	2.73E+08	1.33E+06	7.27E+07
	energy / instruction (relative)			1	5.45E+01
7	energy / clk	J	2.50E-07	3.08E-08	6.67E-08
	energy / clk	fJ	2.50E+08	3.08E+07	6.67E+07
	energy / clk (relative)			1	2.17E+00

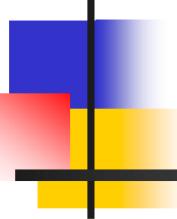
20 kW

optical-processor 80386 (with 300,000 gates)

advantage of serial-processor

latency, synchro issues → 1/100 or less
 programming costs, risks → 1/100 or less
 →→ technical efficiency → 100x / 15 yrs





If anybody likes to keep this talk's slides, please email me!

Summary (ssdm 2010)

- Impacts of ICT-related energy consumptions
 - e.g.: energy supply to Data centers in USA: 10 nuclear reactors
 - heat energy from one server rack: 20-kW level.
- many-folded parallel-data-processes will *the best for all applications*, thru. 2050 ?
- <speed, energy, size> of all-optical gates, at present: <200G, 3 pJ/bit, length, 1 mm>
- <speed, energy, size>, 2nd or 3rd generation: <300G, 0.3 pJ, 250 μm^2 >
- in Materials Research (semi-classical quantum):
 - optical acceleration (incl. gate scheme),
 - electron-photon interaction (little studied),
 - higher-density excitations (w/ larger hetero-barrier).
- optical-4004: MIPS, comparable to Core2 quad. Electric energy, 200W.
- optical-80386: 300,000 gates. Energy per clk, comparable to Core2 quad.
(this will probably save energy and costs, for a group of serial-process-oriented tasks.)



an alternative to 40-year-long Moore's law

Thanks to Co-authors and Collaborations

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