Modeling of the polarization-discriminating-symmetric-Mach-Zehnder-type optical-3R gate scheme and its available degree of random-amplitude-noise suppression

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Abstract: We have modeled the semiconductor-optical-amplifier (SOA) - based polarization-discriminating-symmetric-Mach-Zehnder (PDSMZ) - type (i.e., a UNI-type) 3R gating scheme, and have searched for an optimum set of 3R-gating conditions. Primary parts of the optimum parameters we obtained – such as the interferometer delay time Δt and the widths of input data and clock pulses in the gate model – matched those from previously reported 3R-loop transmission experiments fairly well. We also found that the 3R-gating mechanism which forms the regenerated output signal differs greatly from what it has been thought to be. Based on this model, we have characterized the available degree of random-amplitude-noise suppression.

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1. Introduction

Low-noise, error-free, input-polarization-insensitive optical-3R gating of 80-Gb/s-class pseudorandom data signals has been achieved experimentally [1-3] through use of the polarization-discriminating symmetric-Mach-Zehnder (PDSMZ) semiconductor gate [4] shown in Fig. 1(a). (This PDSMZ gate structure is sometimes called an ultrafast nonlinear interferometer (UNI) [5].) More recently, error-free optical-3R-loop transmission of 40-Gb/s signals with two-cascaded PDSMZ- 3R gates (Fig. 2) was demonstrated by two independent research teams, where the ASE noise that accumulated over each recirculation was clearly suppressed by the PDSMZ-3R gating [6, 7].
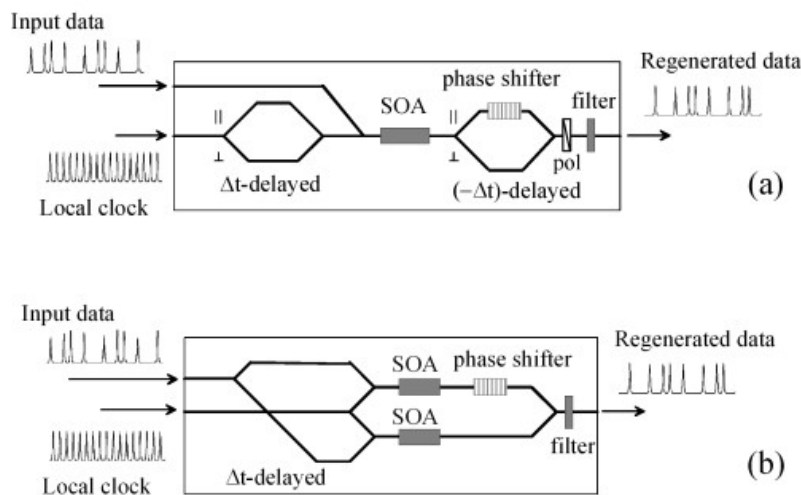

Fig. 1. The two alternative optical-3R gates.

(a) PDSMZ-3R gate [1-3], (b) SMZ-3R gate [8, 9]

Error-free optical 3R gating of 40-Gb/s signals has also been achieved with the SMZ semiconductor gate shown in Fig. 1(b) [8, 9]. In addition, a preliminary theoretical model of this SMZ-3R gating has been reported [10]. However, although this gate structure will be

more suitable than the PDSMZ gate structure for compact integration in the near future [9, 11-13], there have been few reported studies regarding its optical-3R-loop transmission.
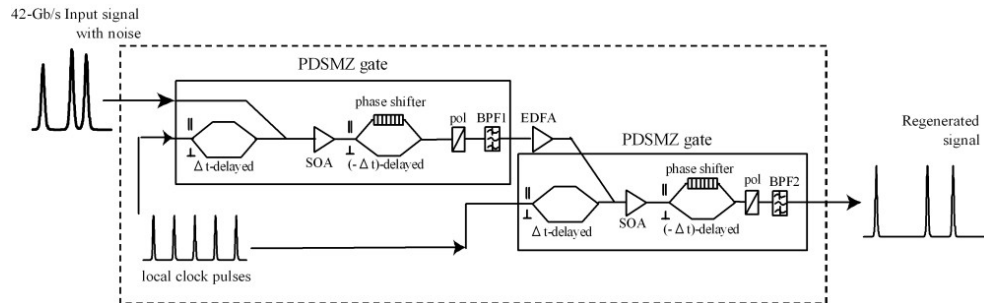

Fig. 2. The optical-3R gate scheme with two-cascaded PDSMZ-3R gates [6, 7].
SOA: semiconductor optical amplifier, BPF1, BPF2: optical band-pass filters, pol: polarizer.

To the best of our knowledge, no theoretical model of the PDSMZ-3R gating mechanism has been reported. In particular, this mechanism's ability to suppress random amplitude noise in the input data signal has never been examined with a reliable model. In addition, the details of the gating mechanism that regenerates the data pulses have never been experimentally characterized, because of the limited time resolution in previous experiments. The gate-window shape, for example, has been thought to be rectangular-like even if the gate is driven by pseudorandom data pulses (Fig. 3), in a manner similar to the mechanism in all-optical SMZ demultiplexing and PDSMZ demultiplexing [4]. The effective width of the gate window has been thought to be close to the delay time Δt in Fig. 3. The gate-window shape in the PDSMZ-3R gating, however, has not been experimentally measured nor theoretically modeled.
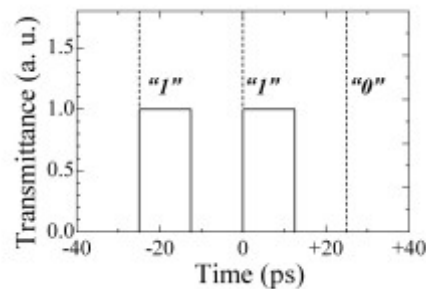

Fig. 3. Conventional PDSMZ-3R gate model.

In this work, we have built the first theoretical model of the PDSMZ-3R gate for characterizing and designing its amplitude-noise-suppression capability. In the modeling processes, we have paid particular attention to two issues:

(1) Because the recovery of the carrier density is accelerated by the input clock pulses, which obviously work as a holding beam [14], the recovery components in the two-split clock pulses seem *not* to be smoothly cancelled after the optical interference inside the gate in a manner similar to that recently reported for the delayed-interferometer signal-wavelength converter (DISC) [15]. How then will an effective gating window be formed and shaped?

(2) The random noise in the logic-zero signal is *not* suppressed so strongly as that in the logic-one signal?

2. Operating principle of the PDSMZ-3R gate scheme

The PDSMZ-3R gate in Fig. 1(a) has been supposed to regenerate the RZ-format data pulses according to the following principle [2, 4]. When each of the input data pulses (which contain random amplitude noise) is amplified by a polarization-insensitive SOA, the carrier density inside the SOA is instantaneously depleted, and then recovered by the dc injection current to the SOA.

On the other hand, the local clock pulses are split into two orthogonally polarized components. After one of the two components is given a delay time Δt, the two components are combined and injected to the SOA. In the SOA, both of the two polarized components are all-optically modulated (i.e., cross-phase modulated and cross-gain modulated), as a consequence of the ultrafast carrier-density oscillation driven by the input data pulses. After the SOA, the two orthogonally polarized components are split into the two respectively polarized components by a polarization splitter, and then the delay time Δt between these two components is compensated for. After the delay-time compensation, the two orthogonally polarized components are combined and filtered by a 45° polarizer. The combined component after the the 45° polarizer is an 'optical-interference component' between the two-split clock-pulse components. Both of the two-split inteference components are cross-phase-modulated and cross-gain modulated in the SOA between the first splitter and the second combiner (i.e. interference combiner), in a manner similar to those in the SMZ-3R gate scheme in Fig. 1(b). The optical interference can be constructive or destructive, depending upon the interference phase bias ΔΦ$_b$ which is optimized by a static optical phase shifter in front of the second combiner in Fig. 1(a).

Each of the clock pulses after the optical interference in the 45° polarizer survives or not, depending upon the binary logic (either 1 or 0) of the co-propagating input data pulses. As a result, the input clock pulses are digitally encoded by the input data pulses, and then reach the output port of the 3R gate as 'regenerated' data pulses. The co-propagating input data pulses are removed by a bandpass filter due to a small difference between the wavelengths of input data and clock pulses, in a manner similar to those in the SMZ-3R gate.

The magnitude of the amplitude noise in the 'regenerated' data pulses has been supposed to be smaller than that in the input data pulses because of the sinusoidal transfer function of the optical interferometer.

3. Our model equations and its validity

The all-optical driving forces in the two-cascaded PDSMZ gates in Fig. 2 consist of the cross-phase modulation (XPM) and cross-gain modulation (XGM) in the two respective SOAs, and the optical interference. In this work, in a manner similar to Ref. 10, the XPM and XGM in each SOA are modeled by the following carrier-density rate equation:

$$\frac{d}{dt}\overline{n_c(t)} = \frac{I_{op}}{qV} - \frac{\overline{n_c(t)}}{\tau_c} - \frac{1}{V} \cdot \left(G\{\overline{n_c(t)}\} - 1 \right) \cdot \frac{\frac{1}{2}|E_{clock}(t)|^2 + \frac{1}{2}|E_{clock}(t-\Delta t)|^2 + |E_{data}(t)|^2}{\hbar\omega}.$$

(1)

Here, $\overline{n_c(t)}$ is the excess carrier density averaged over the propagation distance throughout the SOA chip, I_{op} is the injection current, V is the volume of the active layer, and τ_c is the carrier lifetime. The XGM is expressed as

$$G(t) \equiv \exp[dg/dn_c \cdot \overline{n_c(t)} \cdot \Gamma L],$$

(2)

where Γ is the optical confinement factor and L is the length of the SOA active layer. For simplicity, the differential gain dg / dn_c is assumed to be independent of the carrier density.

The XPM in the optical phases of all propagating light components is expressed as

$$\Phi(t) = -k_0 \cdot dn_r / dn_c \cdot \overline{n_c(t)} \cdot \Gamma L ,\tag{3}$$

where k_0 is the wavevector in vacuum. The nonlinear index of refraction dn_r / dn_c, like dg / dn_c, is assumed to be independent of the carrier density.

The validity of this nonlinear SOA model has been experimentally verified to some extent with output spectra and waveforms from other types of all-optical gates, such as saturated XPM and SPM spectra [16], all-optically demultiplexed waveforms [17], and DISC-type wavelength-converted waveforms [15, 16], mostly in a frequency range from 40 to 160 GHz.

On the other hand, the possible contributions from amplified spontaneous emission and the second-order terms in the gain and the refractive-index as a function of the carrier density were neglected in our model equations. We sacrificed some of the preciseness of our model by neglecting those contributions and keeping our core subroutines compact, so that we could flexibly study these slightly complicated gate schemes. We have also been trying to model and design the performance of these 3R gate schemes to enable *scalable optical-circuit designs* in the near future. We believe this modeling policy of ours will be justified by the above-mentioned, previous series of experimental verifications [15-17].

The pseudorandom input data are modeled as

$$E_{data}(t) = \sum_m \left[C_m \cdot E_m^1 + (1 - C_m) \cdot E_m^0 \right] \cdot \text{sech}(\frac{t - m \times T - t_{tim}}{T_w^{data}}), \text{m} = 1, 2, ..., \infty ,\tag{4}$$

where C_m is the pseudorandom binary code (0 or 1, word length = 2^{31}-1). Independently from the random coding, pseudorandom analog numbers in a normal distribution are also numerically generated and superimposed to the amplitude factor E_m^1 and E_m^0. The pulse shape is assumed to be secant-hyperbolic throughout this work. T is the frame time, t_{tim} is the input timing, and T_w^{data} is a parameter that determines the pulse width.

The amplitude of the uniform input clock pulses is expressed as

$$E_{clock}(t) = \sum_m E_{clock} \cdot \text{sech}(\frac{t - m \times T}{T_w^{clock}}), \text{m} = 1, 2, ..., \infty .\tag{5}$$

The two-split clock pulses after experiencing the XGM and XPM in the SOA are respectively expressed as

$$E_{clock1}^{SOA}(t) = \sqrt{G\overline{\left\{n_c(t)\right\}}} \times \exp\left[i\Phi\overline{\left\{n_c(t)\right\}} \right] \times E_{clock}(t) ,$$

$$E_{clock2}^{SOA}(t) = \sqrt{G\overline{\left\{n_c(t)\right\}}} \times \exp\left[i\Phi\overline{\left\{n_c(t)\right\}} \right] \times E_{clock}(t - \Delta t) .\tag{6}$$

After passing through the SOA, the non-delayed component $E_{clock1}^{SOA}(t)$ is delayed by Δt, is interfered with the previously delayed component $E_{clock2}^{SOA}(t)$, and forms the output *data* pulses as

$$E_{data}^{output}(t) = E_{clock1}^{SOA}(t - \Delta t) + \exp(i\Delta\Phi_b) \cdot E_{clock2}^{SOA}(t)$$

$$= \sqrt{G\{\overline{n_c(t-\Delta t)}\}} \times \exp\left[i\Phi\{\overline{n_c(t-\Delta t)}\}\right] \times E_{clock}(t-\Delta t)$$

$$+ \sqrt{G\{\overline{n_c(t)}\}} \times \exp\left[i\Phi\{\overline{n_c(t)}\} + i\Delta\Phi_b\right] \times E_{clock}(t-\Delta t) \tag{7}$$

$$= T_w(t) \times E_{clock}(t-\Delta t)$$

where $\Delta\Phi_b$ is the optical interference phase bias. The amplitude transmittance of the effective gate window $T_w(t)$ in Eq. (7) is defined as

$$T_w(t) \equiv \sqrt{G\{\overline{n_c(t)}\}} \times \exp\left[i\Phi\{\overline{n_c(t)}\} + i\Delta\Phi_b\right] + \sqrt{G\{\overline{n_c(t-\Delta t)}\}} \times \exp\left[i\Phi\{\overline{n_c(t-\Delta t)}\}\right]. \tag{8}$$

In the conventional manner, the contribution from XPM to the intensity transmittance $|T_w(t)|^2$ is approximated by ignoring the XGM contribution:

$$|T_w(t)|^2 \approx \left| \exp\left[i\Phi\{\overline{n_c(t)}\} + i\Delta\Phi_b\right] + \exp\left[i\Phi\{\overline{n_c(t-\Delta t)}\}\right] \right|^2$$

$$= \cos^2 \frac{(\Delta\Phi(t) + \Delta\Phi_b)}{2}. \tag{9}$$

The optical phase difference between the two-slit interference components $\Delta\Phi(t)$ is defined as

$$\Delta\Phi(t) \equiv \Phi\{\overline{n_c(t)}\} - \Phi\{\overline{n_c(t-\Delta t)}\}. \tag{10}$$

The formulae in Eqs. (8) to (10) are similar to those that have been repeatedly used to describe all-optical SMZ demultiplexing, PDSMZ demultiplexing, and DISC wavelength conversion [16].

4. Calculated results

4.1 Available degree of noise suppression after PDSMZ-type 3R gating

First, we numerically searched for the optimum set of 3R gating conditions; that is, the most suitable parameter values for the PDSMZ-type gates and for the optical inputs. For design simplicity, the conditions for the second gate were expected to be identical to those for the first gate. By testing most of the possible combinations of parameter values, we found that the optimum parameter values, leading to the best output eye diagram, were as summarized in Tables 1 and 2. Primary parts of the optimum parameters, such as the interferometer delay time Δt (Table 1) and the widths of the input data and clock pulses (Table 2), matched those reported from previous 3R-loop transmission experiments fairly well [6, 7]. (Note, though, that the previously reported relative delay time $\Delta t/T$ has ranged from 40% to 61%, as shown in Table 3.)

Table 1. Parameter values for the PDSMZ-gates.

Description	42 Gb/s	168 Gb/s
Unsaturated gain, G_0	28 dB	28 dB
Gain saturation energy, P_{sat}	180 fJ	180 fJ
Carrier lifetime, τ_c	50 ps	12.5 ps
Nominal injection current, I_{nom}	150 mA	600 mA
Enhanced injection current, I_{op}	435 mA	1740 mA
Injection enhancement factor	2.9	2.9

Interferometer delay time, Δt	14.7 ps (61.7%)	3.68 ps (61.7%)
Interferometer phase bias, $\Delta\Phi_b$	1.00π	1.00π
Width of the bandpass filter, $\Delta\lambda_{BPF}$	0.80 nm	3.20 nm
Spectral shape of the bandpass filter	Gaussian	Gaussian

The parameter values for 168-Gb/s data were used later for the results in Fig. 11(b).

The optimum injection current to the SOA in this work was the value of the enhanced injection current in Table 1, in a manner similar to those in Ref. 10. In contrast, the values of the unsaturated gain, the gain saturation energy, and the carrier lifetime in Table 1 were intentionally assumed as those with the nominal injection current in Table 1. [As a consequence, if we assume gating conditions with very weak optical inputs to the SOA, our model calculation outputs unrealistically large carrier density and gain because the gain coefficient in Eq. (2) was assumed to be independent of the carrier density.] When we assumed gating conditions with relatively strong optical inputs such as those in Table 2, both of the carrier density and the gain were saturated and modulated *below* their 'nominal' unsaturated levels which correspond to the nominal injection current. This strong saturation in the 3R scheme was the reason why we defined the injection current in the above-mentioned two ways and why we assumed the gain coefficient and some other parameters nearly constant [10].

Table 2. Parameter values for the optical inputs.

Description	42 Gb/s	168 Gb/s
Input signal's pulse width (FWHM)	6.0 ps	1.5 ps
Input signal's pulse energy	100 fJ	100 fJ
Input signal's pulse shape	sech	sech
Input signal's pulse distance, T	23.82 ps	5.96 ps
Input timing, ΔT_{in}	+2.15 ps (+9.0%)	+0.54 ps (+9.0%)
Q^2 value	19.9 dB	19.9 dB
Input clock's pulse width (FWHM)	3.0 ps	0.75 ps
Input clock's pulse energy	400 fJ	400 fJ
Input clock's pulse shape	sech	sech

Table 3. Comparisons between the relative delay times, $\Delta t/T$.

Gate Scheme	Bit rate (Gb/s)	Delay time Δt (ps)	Time frame T (ps)	Ratio $\Delta t/T$	Ref.
3R gate	80	5	12.5	40%	[1]
Logic gate	40	12.5	25	50%	[5]
Logic gate	100	5	10	50%	a
3R gate	40	12.5	25	50%	b
3R gate	84	6.2	11.9	52%	[2]
Two-cascaded 3R-loop	40	13	25	52%	[6]
3R-loop	40	15	25	60%	c
3R gate	40	15.3	25	61%	b
Two-cascaded 3R-loop	40	15.3	25	61%	[7]
Two-cascaded 3R gate	42	14.7	23.8	62%	This work

(a) K.L. Hall and K.A. Rauschenbach, "100-Gbit/s bitwise logic," Opt. Lett. vol. 23, no. 16, pp. 1271-1273, 1998, (b) M. Tsurusawa, R. Inohara, K. Nishimura and M. Usami, "Operation margin of all-optical regenerator at 40 Gbit/s by SOA-based polarization discriminated switch," Prco. Optical Fiber Communication Conference and Exposition (OFC 2003), Atlanta, USA, Paper ThX3, Mar. 2003, (c) H.J. Thiele, A.D. Ellis, and I.D. Phillips, "Recirculating loop

demonstration of 40 Gbit/s all-optical 3R data regeneration using a semiconductor nonlinear interferometer," Electron. Lett., Vol. 35, no. 3, pp. 230-231, Feb. 1999.
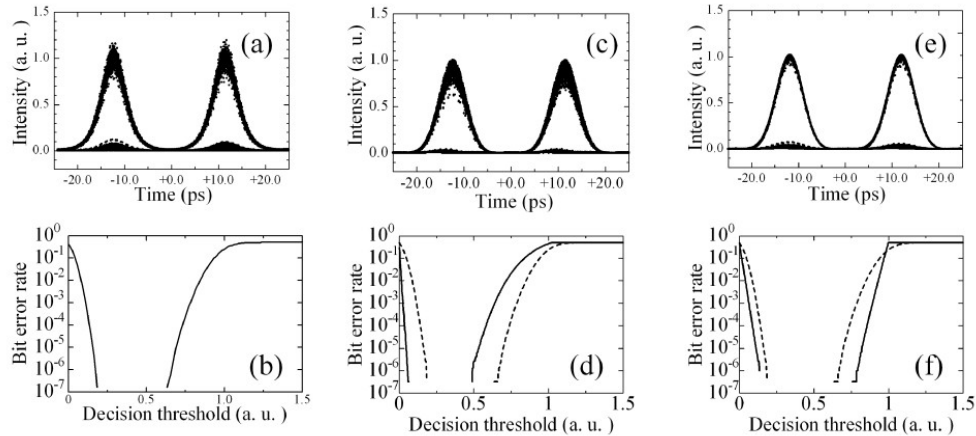
Fig. 4. Calculated 42-Gb/s pseudorandom signals before and after the 3R gating.
(a), (b): Input signal, (c), (d): Intermediate signal after the first PDSMZ gate, (e), (f): Output signal, (a), (c), (e): Eye diagrams, (b), (d), (f): Bit-error rates (BER), Dashed curves in (d) and (f): BER of the input signal in (b), for comparison.

Figure 4 shows calculated eye diagrams and bit-error rates (BERs) before and after the two-cascaded PDSMZ-type gates shown in Fig. 2 when the parameter values from Tables 1 and 2 were used. A 1-kbit-long data pattern was generated to draw the eye diagrams, while a 3-Mbit-long data pattern was generated to calculate the BER curves. The typical calculation time for this set of BER curves with a standard 2.4-GHz personal computer and a standard fast-Fourier-transformation (FFT) library was 34 hours. As shown in Figs. 4(e) and (f), the logic-one-bit noise and the logic-zero-bit noise were both suppressed after the 3R gating. In addition, as shown in Fig. 4(f), the one-bit noise was suppressed more strongly than the zero-bit noise. There are three notable points here:

(1) The range of the one-bit-noise distribution that caused a BER of 10^{-6} in Fig. 4(f) was smaller than it *appeared to be* in the eye diagram in Fig. 4(e). In other words, the statistical BER curve for the regenerated one-bit signals (the solid curve in Fig. 4(f)) was much steeper than for standard one-bit signals with normally distributed noise (e.g., the dashed curve in Fig. 4(f)).

(2) In the intermediate state between the two-cascaded gates, the range of the one-bit noise was expanded rather than suppressed. After the second 3R gate, the expanded one-bit noise was strongly suppressed and was logic-inverted.

(3) The range of the one-bit-noise distribution that caused a BER of 10^{-6} in the output signal was compressed to approximately 62% that in the input. The range of the zero-bit-noise distribution that caused a BER of 10^{-6} in the output signal was compressed to 75% that in the input signal.
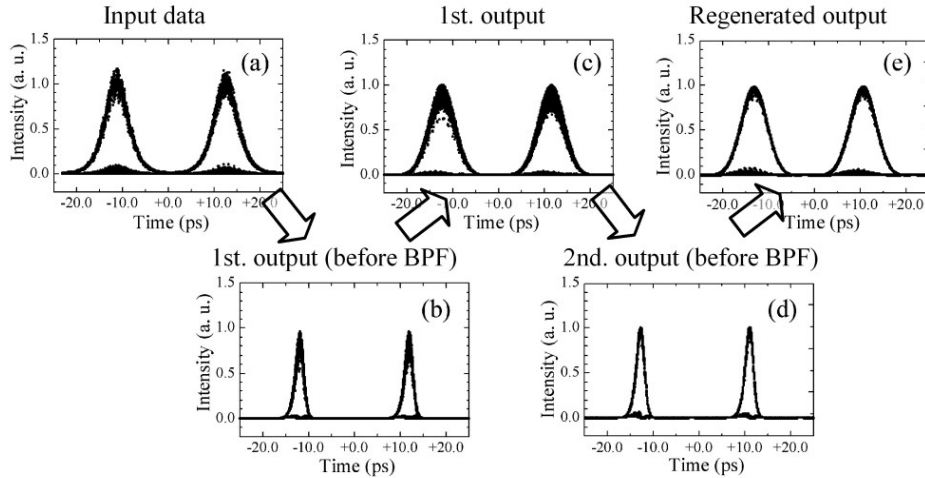
Fig. 5 Transition of 42-Gb/s eye diagrams from the first input to the final output of the two-cascaded PDSMZ-3R gates.

Figure 5 shows the calculated eye diagrams from the first input through the final output in more detail. The width of data pulses in front of BPF1 in the first PDSMZ-3R gate [Fig. 5(b)] was 2.5 ps, which is much narrower than the width of the input data pulses (6.0 ps). When BPF1 was used with a spectral width of 0.80 nm, the width of the data pulses was nearly equalized (6.4 ps) to that of the input data (Fig. 5(c)). The data pulses in front of BPF2 in the second PDSMZ-3R gate [Fig. 5(d)] were narrowed once again. When BPF2 was applied, though, the data pulse's width was again nearly equalized [Fig. 5(e)]. The calculated parameter values of the regenerated data pulses from the two-cascaded 3R gates are summarized in Table 4.

Table 4. Calculated parameter values of the 3R-regenerated data signal.

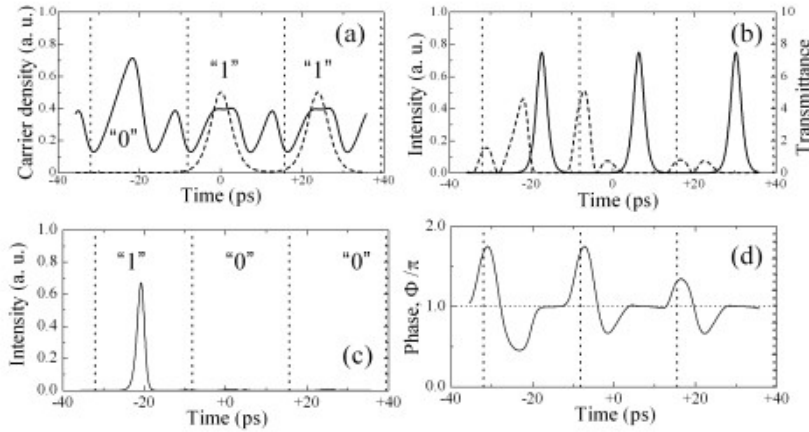| Description	42 Gb/s	168 Gb/s
Output logic	inverted	inverted
Output signal pulse width (FWHM)	6.4 ps	1.6 ps
Output signal pulse energy	3.0 fJ	3.0 fJ
Q^2 value	29.4 dB	29.4 dB
Minimum bit-error rate	$< 10^{-6}$	$< 10^{-6}$
Nonlinear phase shift, $\Delta\Phi_{NL}$	0.36π	0.36π

Fig. 6. Physical mechanism that regenerates the 42-Gb/s patterned data pulses.(a) Carrier-density oscillation (solid), induced by both '011' input data (6.0 ps) and clock pulses, (b) Effective gate-window's transmittance $T_w(t)$ (dashed), with respect to the delayed clock pulses (3.0 ps, solid), (c) Logic-inverted '100' output data pulses (before being bandpass-filtered), (d) Trace of the difference between the optical phases of the two-split clock-pulse components

Figure 6 shows the physical mechanism inside the first PDSMZ gate according to our calculation. According to the rate equation (Eq. (1)), the carrier density in the SOA [Fig. 6(a)] was instantaneously depleted by three types of input pulse: the '011' data pulses [dashed curve in Fig. 6(a)], the clock pulses, and the Δt-delayed orthogonally polarized clock pulses. The dotted vertical lines in Figs. 6(a) to (d) indicate the positions of non-delayed clock pulses. Figure 6(b) shows the transmittance of the effective gate window $\left|T_w(t)\right|^2$ (Eq. (8)), with respect to the Δt-delayed clock pulses $\left|E_{clock}(t-\Delta t)\right|^2$.

Figure 6(c) shows the output data waveform $\left|E_{data}^{output}(t)\right|^2$ in front of the BPF1, which was generated from the overlaps $T_w(t)\times E_{clock}(t-\Delta t)$ between the effective gate-window waveform and the delayed-clock-pulse waveform in Fig. 6(b), according to Eq. (7). In the example shown in Fig. 6, the input data code was '011' and the logic-inverted output data code was '100'. As in Figs. 5(b) and (d), the output pulse in Fig. 6(c) was greatly narrowed. Figure 6(b) indicates that this pulse narrowing was caused by the width of the corresponding overlap between $T_w(t)$ and $E_{clock}(t-\Delta t)$.

Note that the effective gate-window waveform $\left|T_w(t)\right|^2$ in Fig. 6(b) significantly differs from what it had previously been thought to be; that is, rectangular-like waveforms (Fig. 3). Furthermore, Fig. 6(d) shows the time evolution of the temporal optical phase difference $\Delta\Phi(t)$ in Eq. (10), indicating that the contribution from XPM to the 3R-gate-window waveform differed significantly from that of the SMZ demultiplexing in Eq. (9).

The magnitude of the so-called nonlinear phase shift $\Delta\Phi_{NL}$ that is visible in Fig. 6(d) has been recognized as one of the most important gating conditions in all interferometric types of all-optical semiconductor gates (e.g., [16]). In the case of our PDSMZ-3R gating, we defined $\Delta\Phi_{NL}$ as the temporal phase shift from 1.0π *at the time of the output pulse's peak position*. According to this definition, $\Delta\Phi_{NL}$ in Fig. 6(d) was 0.36π (Table 4).
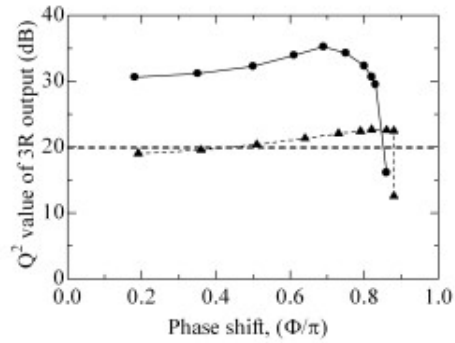
Fig. 7. Dependence on the magnitude of the nonlinear phase shift, $\Delta\Phi_{NL}$ solid curve: Q^2 of the output signal after the two-cascaded PDSMZ gates, dashed curve: Q^2 of the intermediate signal between the two-cascaded 3R gates, dashed line: Q^2 of the input signal.

Although the phase shift required for full switching from destructive to constructive interference (or vice versa) in a Mach-Zehnder interferometer is 1.0π, the $\Delta\Phi_{NL}$ value in Fig. 6(d) was much smaller than $1.0\,\pi$. In a calculation whose results are shown in Fig. 7, we temporarily assumed larger and smaller dn_r/dn_c values and investigated how the resultant larger and smaller $\Delta\Phi_{NL}$ values would consequently affect the noise suppression capabilities. According to our calculation, the noise was suppressed slightly more as $\Delta\Phi_{NL}$ approached 0.7π (Fig. 7). When $\Delta\Phi_{NL}$ was increased to more than 0.7π, the output data waveform was distorted and consequently the Q^2 value of the output signal started dropping. Thus, unexpectedly, we found that $\Delta\Phi_{NL}$ of $1.0\,\pi$ is too large for the PDSMZ-3R gating.

4.2 Possible output distortions and their respective origins

When one of the gating parameters is adjusted too far beyond its tolerance range, the output waveform will obviously be distorted. Figures 8(a) and (b) show two types of such output-waveform distortion, while Fig. 8(c) shows the waveform with very little distortion under the optimum conditions.
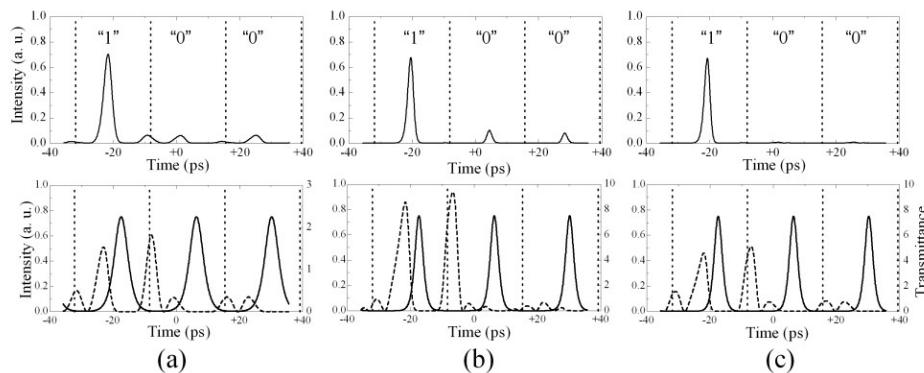

Fig. 8. Possible output-waveform distortions. Upper: output waveforms, lower: gating windows (dashed) with respect to the input clocks (solid), (a) Asynchronous clock leakage, when the clock pulse's width is too broad, (b) Synchronous clock leakage, when the clock power is too weak, (c) Little distortion, when the conditions of the input clock are acceptable.

The waveform distortion in Fig. 8(a) occurred when the width of the secant-hyperbolic clock pulses was broadened to 5.0 ps from the optimum value of 3.0 ps (Table 2). Three separate leakage components can be clearly seen, which were generated by three unexpected

overlaps between the gating window and the input clock components. One of the three leakage components was asynchronous and the other two were nearly synchronous to the data pulse positions.

The waveform distortion in Fig. 8(b) occurred when the energy of the input clock pulse was decreased to 100 fJ from its optimum value of 400 fJ. Two separate leakage components can be seen, which were generated by two unexpected overlaps between the gating window and the input clock. Both of these leakage components were nearly synchronous to the data pulse positions.

We expect the clear difference between the leakage positions in Figs. 8(a) and 8(b) to be useful for diagnosing such forms of output waveform distortion in experimental 3R research. Our calculated results in Fig. 8 suggest that when leakage components are synchronous to the data positions, they can be removed by increasing the input clock power; when one of the leakage components is asynchronous to the data positions, it can be removed by narrowing the width of the input clock pulses.

4.3 Tolerance to the input data pulse width and the input timing

We chose to use input secant-hyperbolic data pulses whose full width at half maximum (FWHM) was 6.0 ps (Table 2), narrower than the more common FWHM (10-12 ps) of data pulses used in recent RZ-formatted transmission experiments. We therefore investigated the dependence of the noise suppression capability on the width of input data pulses at about 6.0 ps (Fig. 9). The decision threshold limits in the figure were defined as the upper and lower limits of the decision-threshold range where the calculated BER reached 10^{-6}. The PDSMZ-3R gating tolerated a width of approximately 8 ps (Fig. 9). As the width of the data pulses increased from 6 ps, the noise in the logic-one signals was slightly less suppressed. In contrast, the noise in the logic-zero signals was not very dependent on the data pulse width. We speculate that the tolerance in Fig. 9 may be broadened when we study this using Gaussian data pulses.
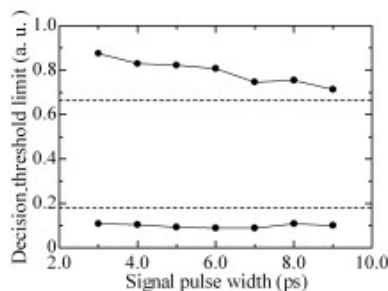

Fig. 9. Dependence of the decision-threshold limits on the width of the input signal. The decision-threshold limit in this work is defined as a limit of the decision-threshold level where the bit-error rate reaches 10^{-6}.

We also studied the BER tolerance with regard to the input timing of 42-Gb/s data pulses with 6.0-ps data pulses and the other optimum conditions from Tables 1 and 2. The width of the tolerance range for the input timing in this work was approximately 4 ps (Fig. 10).
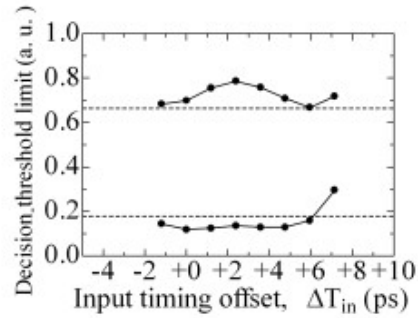
Fig. 10. Dependence on the signal's input timing.

4.4 Frequency-scaling rule

Our final step in this work was to numerically test whether the PDSMZ-3R gate would follow the frequency-scaling rule that one of us analytically proposed and numerically verified with respect to the SMZ-3R gate model [Fig. 1(b)] [10]. As was mentioned earlier in the text, our goal is to enable scalable optical-circuit design. According to the frequency-scaling rule given in [10], we can quadruple, for example, the frequency of any type of 3R gating result if we can scale the gate and input parameter values given in Tables 1 and 2 as follows: (1) narrow the widths of the signal and clock pulses by a factor of 4, (2) maintain the energies of the signal and clock pulses, (3) shorten the carrier lifetime of the SOA(s) by a factor of 4, (4) increase the carrier injection by a factor of 4, (5) maintain the injection enhancement factor, and (6) shorten the interferometer delay time by a factor of 4.

In this work, we calculated eye diagrams before the frequency-scaling (42 Gb/s) and after the frequency-scaling (168 Gb/s), using the respective parameter values in Tables 1 and 2. As a result, the frequency-scaled eye diagram which contained the compressed amplitude noise completely matched the eye diagram before scaling. Thus, we have numerically verified the frequency-scaling rule for the PDSMZ-3R gate.

5. Conclusion

We have modeled the semiconductor-optical-amplifier (SOA) -based polarization-discriminating-symmetric-Mach-Zehnder (PDSMZ) -type (i.e., a UNI-type) 3R gating scheme, and have searched for an optimum set of 42-Gb/s 3R-gating conditions. Primary parts of the optimum parameters, such as the interferometer delay time Δt (62% of the frame time, T) and the widths of input data (6 ps) and clock pulses (3 ps) in the gate model, matched those from previous 3R-loop transmission experiments fairly well. We also found that the 3R-gating mechanism which forms the regenerated output signal differs dramatically from what it was thought to be.

Based on this new model, we characterized the available degree of random-amplitude-noise suppression. The compression ratio of the noise distribution range (calculated at a BER level of 10^{-6}) in the logic-one signal was approximately 62%, and that in the logic-zero signal was 75%. We also investigated the dependence of the noise-suppression capability on several 3R-gating conditions, such as the required nonlinear-optical phase shift $\Delta\Phi_{NL}$ inside the gate and the widths of the signal and clock pulses.

These modeling results will provide basic guidelines for optical-3R transmission research and for more fundamental 3R gating experiments.